CHAPTER 8

OVERVIEW OF EMBEDDED SOC SYSTEMS

The remainder of the book applies the basic hardware design techniques learned in Part I to develop a simple and functional *embedded SoC (System on a Chip)* that contains a video subsystem and a memory-mapped I/O subsystem with general-purpose peripherals, customized hardware accelerators, and a music synthesizer. Our study is still focusing on the hardware design, but within the context of SoC, and it introduces many important design concepts, such as hardware acceleration, bus interface, and software drivers, along the way. In this chapter, we introduce the concept of an embedded SoC, discuss the development flow, explain the simple SoC framework used in this book, and provide an overview of Parts II, III, and IV.

8.1 EMBEDDED SOC

8.1.1 Overview of embedded systems

An *embedded system* (or *embedded computer system*) can be loosely defined as a computer system designed to perform one or a few specific tasks. The computer system is not the end product but a dedicated "embedded" part of a larger system that often includes additional electronic and mechanical parts. By contrast, a *general-purpose computer system*, such as a PC (personal computer), is a general computing platform and itself is the end product. We refer to it as a *desktop-like computer system* in the book. A desktop-like system is designed to be flexible and

to support a variety of end-user needs. Application programs are developed based on the available resources of the general-purpose computer system.

Embedded systems are used in a wide range of applications and each application has its own specific requirements. On one hand, a "low-end" system, such as a microwave oven, involves only a simple control function and can be implemented by an 8-bit single-chip microcontroller. On the other hand, a "high-end" system, such as a digital camera, is more complex. It performs two major tasks. The first task involves the general "housekeeping" I/O operations, including processing the button and knob activities, generating a menu on an LCD display, and writing image files to the storage device. These operations are more involved than those of a microwave oven and the system requires a more capable processor. The second task is to process the image and perform data compression to reduce the file size. Because of the large number of pixels and the complexity of the compression algorithm, the task requires a significant amount of computation. An embedded processor is usually not powerful enough to handle the computation-intensive operation. A custom digital circuit, sometimes known as a *hardware accelerator*, can be designed to perform this particular task and take the load off the processor.

8.1.2 FPGA-based SoC

A "high-end" embedded system usually has a processor and simple I/O peripherals to perform general user interface and housekeeping tasks and special hardware accelerators to handle computation-intensive operations. These components can be integrated into a single integrated circuit, commonly referred to as an *SoC* (*system on a chip*).

As the capacity of FPGA devices continues to grow, the same design methodology can be realized in an FPGA chip. Instead of just realizing the system functionalities by *customized software*, we can incorporate *customized hardware* into the embedded system as well. The FPGA technology allows us to tailor the processor, select only the needed I/O peripherals, create a custom I/O interface, and develop specialized hardware accelerators for computation-intensive tasks. The FPGA embedded system provides a new dimension of flexibility because both the hardware and software can be customized to match specific needs. The methodology of exploiting the trade-offs between hardware and software and developing and integrating them concurrently is referred to as *hardware-software co-design*.

8.1.3 IP cores

In SoC development, systems frequently have certain common functionalities and the same building blocks can be reused in different designs. These components are known as *IP (intellectual property) cores*, or simply as *IPs*. They are somewhat like functions in a software library, which can be used in different application programs. The IP cores can be developed by the device manufacturers, third-party vendors, or the users themselves. Unlike software functions, FPGA vendor's IP cores are usually tailored for their own proprietary platforms. They are not portable and frequently delivered as "black boxes" (i.e., without HDL source codes). For example, all companies provide FFT (fast Fourier transform) IP cores. While the cores perform similar functions, their interfaces, timing characteristics, and configuration

procedure are different. Therefore, a system must be redesigned or modified if it is re-targeted to a device from a different vendor.

8.2 DEVELOPMENT FLOW OF THE EMBEDDED SOC

The embedded SoC design consists of the following tasks:

- Partition the tasks to software routines and hardware accelerators.
- Design user custom IP cores if needed.
- Develop the hardware.
- Develop the software.
- Implement the hardware and software and perform testing.

These tasks are discussed in the following subsections.

Because of the complexity of modern digital systems, pre-designed IP cores are used extensively in SoC development. Each vendor has its own IP framework, which provides a comprehensive collection of IP cores and supporting software device drivers. The development flow is frequently centered on the IP cores and is shown in Figure 8.1.

8.2.1 Hardware–software partition

Step 1 (labeled 1 in the diagram) is to determine the software–hardware partition. An embedded application usually performs a collection of tasks. In an SoC-based design, a task can be implemented by hardware, software, or both. Based on the performance requirement, complexity, and hardware core availability, we can decide the type of implementation accordingly.

In an ideal scenario, the vendor IP library contains all the needed IP cores for the SoC design. However, in reality, most designs require a certain number of custom IP cores for hardware accelerators and special I/O peripherals. Step 2 is to develop the hardware codes and the corresponding software drivers of these custom IP cores. The details are discussed in Subsection 8.2.5.

8.2.2 Hardware development flow

The left branch represents the hardware design flow. Step 3 is to utilize and integrate the IP cores to construct the system. In Vivado Design Suite, it is done by the IP integrator utility. A user can select IP cores, configure them with the desired characteristics, and connect the cores with a proper interface. IP Integrator will invoke the cores from the library and generate the HDL codes. The top-level HDL file usually resembles the top-level block diagram of an SoC design. During the generation, IP Integrator also produces an auxiliary *hardware platform specification file*, which contains the "definition" of the SoC design, including the processor configuration, memory size and structure, I/O peripheral cores used, memory address mapping, etc.

The top-level HDL file can be treated as a normal HDL file and processed accordingly. Steps 4 and 5 perform synthesis and placement and routing and eventually generate the FPGA configuration file (i.e., the `.bit` file).

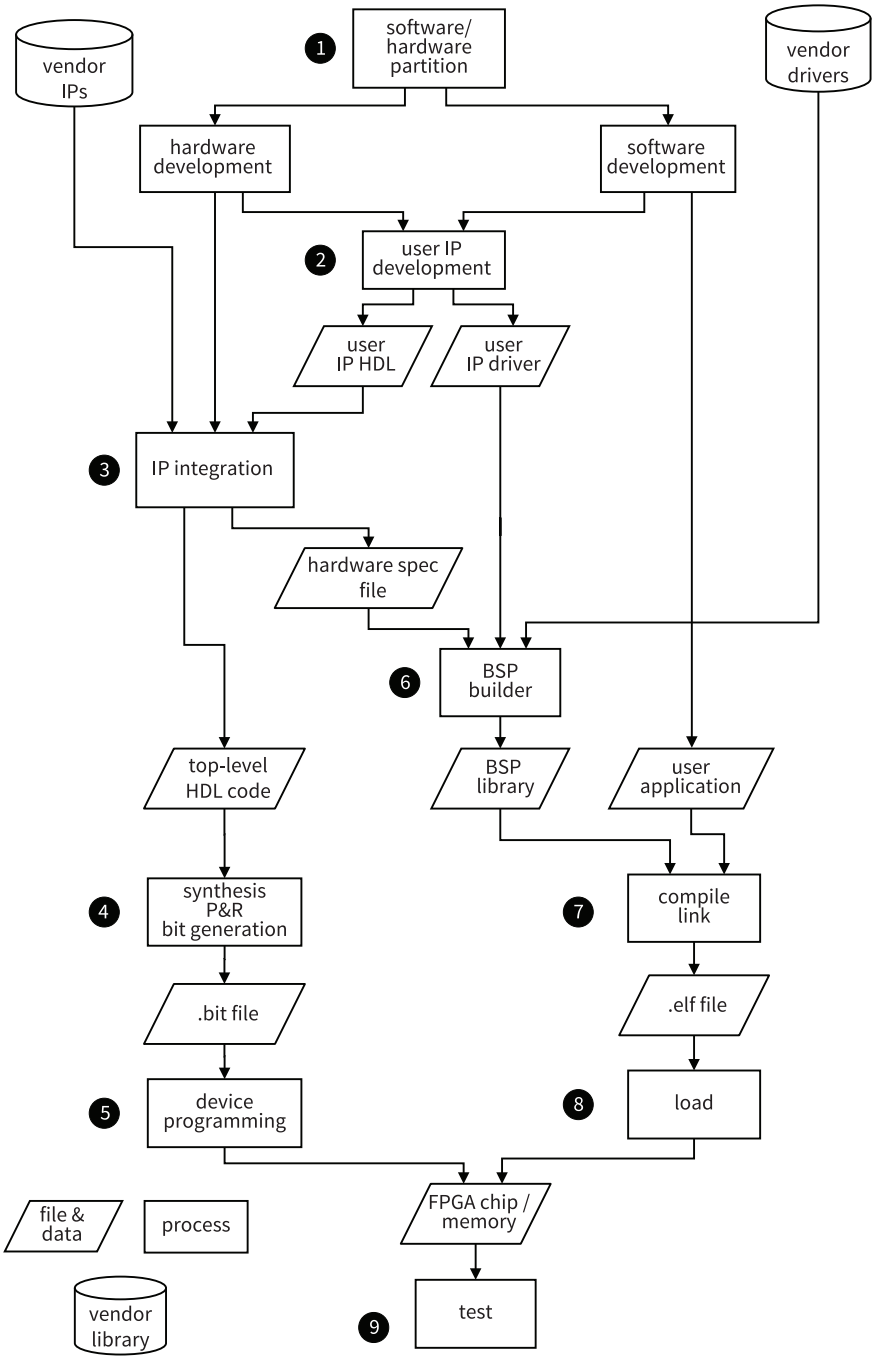

Figure 8.1 IP-centered SoC development flow

8.2.3 Software development flow

The right branch represents the software design flow. A top-level software program usually contains two types of codes. One type is the "system codes," which are pre-designed and provided with the system. They can be functions from libraries, service routines from the operating system, etc. The other type is the "application codes," which are developed by the user to perform the custom tasks. These system functions and service routines are called by the application codes.

In an embedded system, a *BSP (board support package)* is a mechanism to encapsulate the system codes. Since an embedded system is designed to perform a specific task, each system has a different memory structure and contains a unique set of I/O peripherals. BSP is a customized collection of device drivers and initialization routines that support a particular system. The term "board" is used since earlier embedded systems were implemented in a printed circuit board rather than a single silicon device.

An important ingredient of a BSP is the *device drivers*. A device driver is a set of routines that operate or control a particular peripheral device. A driver acts as a "translator" between the hardware peripheral and application programs and enables the application programs to access peripheral functions without needing to know precise details. If an IP core is expected to interface with a processor, a device driver should be developed concurrently.

The embedded SoC flow adopts the BSP mechanism. Step 6 is to build the BSP according to the SoC hardware configuration. Recall that, in Step 3, IP integrator generates a hardware platform specification file. The BSP builder utility examines the IP core information, extracts the pre-build device drivers and initialization routines from the vendor software library, and creates the BSP for the specific SoC design.

The application program can invoke the driver routines in the BSP to access the peripheral I/O cores. Step 7 compiles and links the software routines and BSP library and builds the final software image file (i.e., the .elf file).

8.2.4 Physical implementation and test

Physically implementing the system involves two steps. We first download the FPGA configuration file to the FPGA device (i.e., "program" the device), as in Step 5, and then load the software image into processor's main memory, as in Step 8. The physical system can be tested afterward, as in Step 9.

8.2.5 Custom IP core development

Although FPGA vendors provide a comprehensive collection of pre-designed IP cores, they seldom can cover all the project needs. We usually have to design custom IP cores for special I/O peripherals or less common computation algorithms. The development consists of three tasks:

- Design a custom digital circuit to implement the computation algorithm or special functionality.
- Derive an interface to connect the circuit to the bus or interconnect structure of the vendor's IP framework.

- Develop a device driver to control the new hardware core and integrate it into vendor's software library.

Note that the latter two activities depend on the FPGA vender's IP platform. We need to carefully study the platform's interface protocols and driver structure so that the IP core can be integrated into vendor's framework and used in the IP integration utility. Since each vendor has its own proprietary IP platform, the interface and driver are not portable and must be re-designed for each vendor.

8.3 FPRO SOC PLATFORM

8.3.1 Motivations

While the embedded SoC is powerful methodology, it is not the emphasis of this book. First and foremost, this book focuses on the register-transfer level hardware design rather than the system-level analysis and integration. In addition, a commercial IP platform is not ideal for learning introductory hardware design for several reasons:

- A commercial IP platform is quite complex and thus a significant amount of time will be spent on learning to use the tool rather than doing design.
- Most commercial IP cores are provided as black boxes.
- The interface protocol and driver structure are quite complex.
- The IP framework is proprietary. Thus, learning is tied to a particular platform and the developed IP cores are not portable.

In this book, we define a simple SoC platform and call it *FPro SoC*, (which is abbreviated from the book title "FPGA Prototyping" or can be interpreted as "Fun and Professional"). It contains a video subsystem and a memory-mapped I/O subsystem with general-purpose peripherals, customized hardware accelerators, and a music synthesizer. Our study is still focusing on the hardware design but within the SoC context. The main characteristics of the FPro SoC platform are as follows:

- *Simple.* The FPro SoC platform defines a simple synchronous bus protocol and a straightforward device driver structure. Once a hardware circuit is developed, it can be converted to an IP core by adding a simple interface circuit and a device driver. The core then can be incorporated into the existing embedded system.
- *Functional.* FPro SoC platform provides a variety of I/O peripherals and commonly used serial interfaces (UART, SPI, and I^2C) and includes working device drivers. It resembles a bare-metal 32-bit microprocessor board and can implement real-world projects targeted for this type of boards.
- *Portable.* Except for the processor, FPro SoC's IP cores are developed from scratch in HDL and do not use any vendor's proprietary components. The bus protocol and device drivers are not tied to any specific commercial platform, either. Thus, the IP cores and software codes are portable and can be reused for different FPGA devices and prototyping boards.
- *"Upward compatible."* While the FPro SoC platform is simple, the development follows rigorous and proven design principles and practices. These knowledge and skills can be applied in the future for more complicated commercial platforms and larger projects. In fact, the IP cores and drivers devel-

oped can be easily modified to be incorporated into existing commercial IP frameworks.

- *Fun.* Because the developed system is like a real microprocessor board, it can incorporate existing I/O modules and quickly develop a functional prototyping project. In addition, this platform can provide hardware acceleration capability and thus is more capable and more flexible than any microprocessor board. This give us an opportunity to develop interesting and challenging projects and make studying hardware more "fun" rather than "learning hardware for the sake of hardware."

8.3.2 Platform hardware organization

The top-level diagram of an FPro system is shown in Figure 8.2. It is composed of four major parts:

- Processor module
- FPro bridge and FPro bus
- MMIO (memory mapped I/O) subsystem
- Video subsystem

We only use vendor's IP cores for the processor, memory controller, line buffer, and clock management circuit, which are shown as dotted gray boxes in the figure, and construct all other cores from scratch.

Processor module The processor module consists of a processor, a memory controller core, and RAM. It is the part that is constructed from the vendor's IP cores. To be used in the FPro SoC platform, the processor core must exhibit the following characteristics:

- 32-bit-wide data path
- 32-bit memory address space
- *Memory-mapped-I/O* scheme for I/O access

Almost all FPGA-based processors support these features. There is no restriction on types of RAM. It can be FPGA's internal memory modules or external memory devices. However, since an FPro system resembles an entry-level 32-bit embedded system, we assume that the size of RAM is limited and software is developed in this context.

FPro bridge and FPro bus The processor needs to communicate with other cores. This is done by a *bus* or *interconnect structure* specified in the vendor's IP platform. The modern interconnect is designed to accommodate a wide variety of communication and data transfer needs and involves complex protocols. For our learning purposes, we define a simple synchronous bus protocol for the two subsystems and call it *FPro bus*. The *FPro bridge* converts vendor's native bus signals into FPro bus signals. The FPro bus protocol and bridge are discussed in Chapter 10.

MMIO subsystem In the memory-mapped-I/O scheme, the memory and registers of the I/O peripherals are mapped to the same address space. This means that the processor makes no distinction between the memory and I/O peripherals and uses the same read and write instructions to access the I/O peripherals.

The MMIO subsystem provides a framework to accommodate memory-mapped general-purpose and special I/O peripherals as well as hardware accelerators. For

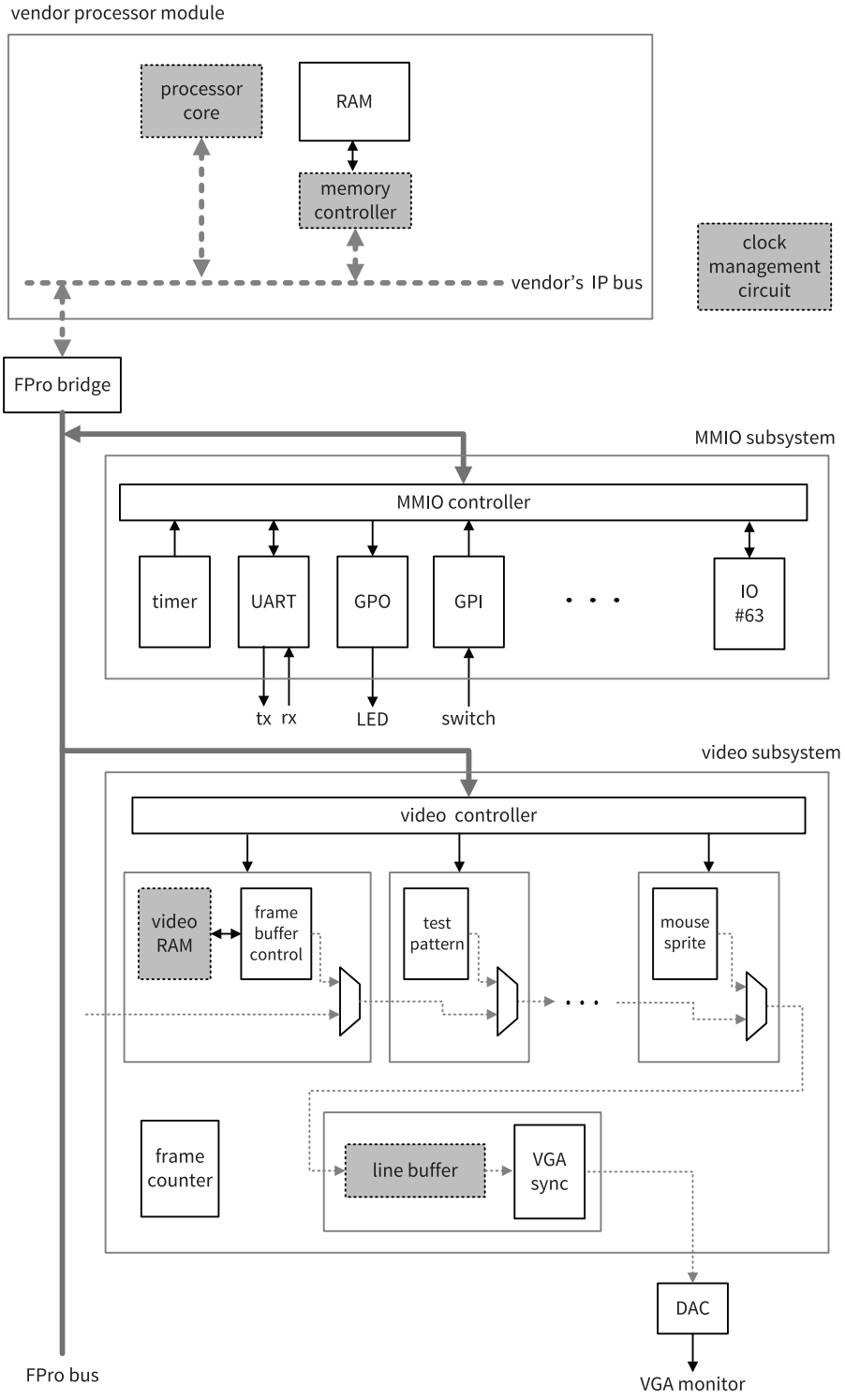

Figure 8.2 Top-level diagram of an FPro system

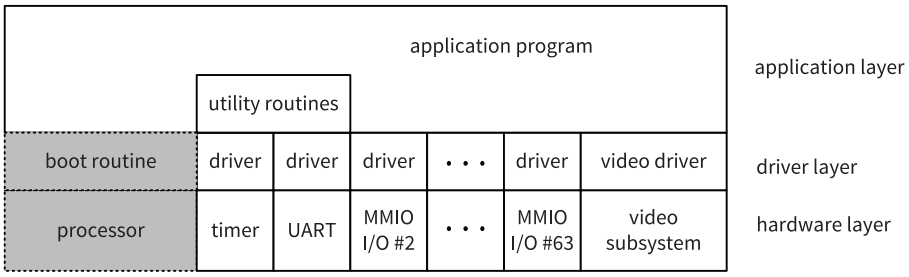

Figure 8.3 Software hierarchy of an FPro SoC system

simplicity, we define a standard *slot interface* that conforms to the FPro bus protocol. The MMIO subsystem consists of a controller to select a specific slot and can accommodate up to 64 instantiated cores. After being "wrapped" with an interface circuit, custom digital logic can be plugged into the FPro platform. About a dozen IP cores are developed and integrated into the MMIO subsystem in the subsequent chapters.

Video subsystem The video subsystem establishes a framework to coordinate the operation of video cores. A video core generates or processes the video data stream. The cores are arranged as a cascading chain. The data stream is pipelined and "blended" through each stage and eventually displayed on a VGA monitor. The video subsystem demonstrates the principles of handling *stream data*, in which data are generated continuously and passed through a chain of components for processing.

8.3.3 Platform software organization

Since the book focuses on hardware design, we use a simple *bare metal* software scheme for the system. A bare metal system contains no operating system. In its simplest form, the processor boots directly into an infinite main loop, which contains functions to check input, perform computation, and write outputs.

The software hierarchy of an FPro system is shown in Figure 8.3. It contains a *hardware layer*, a *driver layer*, and an *application layer*. A *boot routine* is associated with the processor. It first performs the basic initialization process, such as clearing the caches, configuring the stack and heap segments, and initializing the interrupt, and then transfers control to the main program. The codes are obtained from the vendor, as shown in a dotted gray box in the figure. All other device drivers are constructed from scratch.

To facilitate the software development, we develop several simple utility routines that maintain a system time and assist displaying a debug message on the console. The timer core and UART (universal asynchronous receiver and transmitter) core in slots 0 and 1 are used for this purpose, as shown in Figure 8.2. Thus, the two cores should always be instantiated in the first two slots and not be replaced.

Every I/O core in the FPro system is accompanied by a driver. We select C++ for driver development because of its support of data encapsulation. A C++ class will be created for each core.

Except for accessing system time (via a timer core) and sending debugging messages (via a UART core), a class is largely "self-contained" and does not interact with other classes. When a core is attached or removed from an FPro system, the corresponding driver files should be included or deleted from the software projects. In the main application program, an instance will be created for each instantiated IP core and the methods in the class will be used to access and control the core. The "state" of the core, if existing, is kept within the private section of the instantiated object and involves no external variables.

8.3.4 Modified development flow

The original development flow shown in Figure 8.1 needs to be revised to accommodate the FPro SoC platform. While the basic procedure remains unchanged, we need to manually construct the top-level HDL code and manually include the device driver files in our software application. The modified flow is shown in Figure 8.4 and the new paths are highlighted as thick gray dotted lines in the top half. The main changes are as follows:

- In Step 3, only the processor module, which contains a processor core and RAM, is generated via the IP integration utility. We must manually construct the HDL code for the top-level system, which is composed of the instantiation of the previously generated processor module and the MMIO and video subsystems from Step 2.
- In Step 6, since only the processor module configuration is listed in the hardware specification file, only processor-related codes, such as the boot routine, will be included in the BSP library. We must manually examine the IP cores in the top-level HDL file and include the corresponding driver files in the application software project.
- Since the processor module is the same most of the time, Steps 1 and 6 only need to be executed once. The generated HDL files and BSP library can be use in subsequent designs.

8.4 ADAPTATION ON THE DIGILENT NEXYS 4 DDR BOARD

The book uses the Digilent Nexys 4 DDR prototyping board, which is designed around the Xilinx Artix 7 XC7A100T device, for the experiments and projects. Xilinx provides a soft-core processor, known as *MicroBlaze*, as well as a completely "pre-configured" system, known as *MicroBlaze MCS* (for *MicroBlaze Micro Controller System*). We select MCS as the processor module in Figure 8.2.

MicroBlaze is a 32-bit FPGA-based processor with RISC (reduced instruction set computer) architecture. It is highly configurable and can incorporate an optional floating-point unit, instruction and data caches, a memory management unit, etc. MicroBlaze mainly uses the *AXI (Advanced eXtensible Interface)* protocols from ARM to interface with other IP cores. Hundreds of IPs from Xilinx and third-party vendors, including memory controllers, I/O peripherals, and various types of hardware accelerators, can be integrated with a MicroBlaze to form an SoC design. The flow in Figure 8.1 is targeted for this type of setting.

MicroBlaze MCS is a *complete computer system* that is composed of a pre-configured MicroBlaze processor, a RAM constructed with FPGA's internal mem-

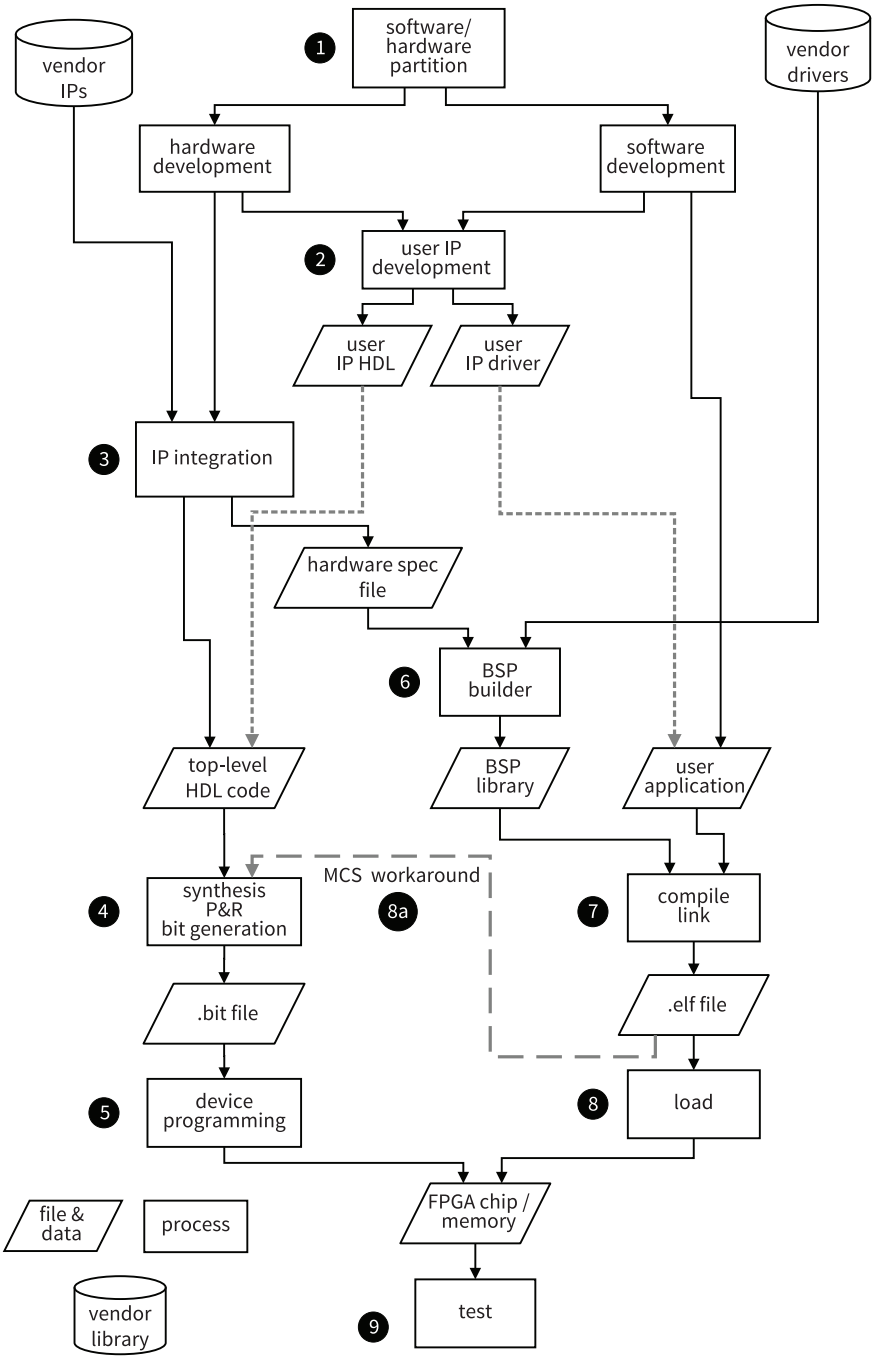

Figure 8.4 FPro SoC development flow

ory, and an I/O module with a standard set of microcontroller peripherals. MicroBlaze MCS provides only a limited degree of configurability. A user can set the size of RAM (between 8 KB and 128 KB) and select a small set of simple I/O peripherals.

Since the focus of the book is hardware design rather than system-level integration, MicroBlaze MCS serves the purpose very well. In addition, many simpler prototyping boards use Xilinx's earlier Spartan devices and must use ISE WebPack for development. At the time of writing, MicroBlaze MCS is free across all Xilinx platforms, including both the ISE WebPack edition and Vivado WebPack edition, but the full-featured MicroBlaze processor is only free for the Vivado WebPack edition. Thus, MicroBlaze MCS can be adopted by more entry-level prototyping boards.

On the down side, support for MicroBlaze MCS is not as comprehensive. The Vivado 2016 edition is used at the time of writing. Step 8 in Figure 8.4 does not function properly. The workaround is to associate the `.elf` file as the "initial values" of FPGA's internal memory and regenerate the configuration file (i.e., `.bit` file). The approach is shown as a thick dashed line in the bottom of Figure 8.4. The revised flow becomes:

- Develop and implement hardware (Steps 1 to 4).
- Develop and implement software (Steps 2 to 7).
- Associate the `.elf` file in the hardware project (Step 8a.).
- Regenerate the configuration `.bit` file with the embedded `.elf` file (i.e., repeating Step 4).
- Program the FPGA device and perform testing (Steps 5 and 9).

This flow is less ideal since regenerating the `.bit` file for each software revision is time-consuming and Vivado software must be invoked during software development.

XC7A100T is a fairly large device and its internal memory modules can accommodate 128 KB RAM for MicroBlaze MCS and 350 KB video RAM for a 9-bit VGA frame buffer. Thus, no external memory device is involved.

8.5 PORTABILITY

A main goal of this book is to develop a portable system to learn hardware design and to introduce SoC practice. Because of the proprietary development software, the IP platform, and IP cores, it is difficult to construct a complete device- and board-independent FPGA-based SoC system. The experiments and projects in this book are constructed and tested on a specific board (Digilent Nexys 4 DDR) that contains a specific FPGA device (Xilinx Artix 7 XC7A100T). The following subsections discuss portability issues.

8.5.1 Processor module and bridge

Since the processor module is constructed from the vendor's proprietary IP cores, it potentially introduces several portability issues:

- Processor
- Memory controller and RAM
- Interface and bridge
- Loading and booting of software

The FPro platform basically requires a 32-bit processor core that supports memory-mapped I/O scheme. Almost all FPGA-based processors satisfy this requirement. The internal and external memory sizes and configurations can vary significantly among different FPGA devices and prototyping boards. However, since the RAM inside the processor module only interacts with the processor core, it does not affect the subsystems directly. In summary, although the proprietary and different memory configurations are used in the processor module, they will not cause serious compatibility issues. The simplest way to create the processor modules is to utilize FPGA's internal memory, as in MicroBlaze MCS. However, older and simpler FPGA devices provide less internal memory. MicroBlaze MCS can be configured with smaller RAM. The size of the RAM, of course, sets the limit on the size of application program.

The FPro bus protocol is designed for simple non-burst synchronous read and write transactions. It can be considered as a very small subset of existing full-featured bus interfaces. Designing a bridge is not very difficult.

While compiling and linking the software code follows a similar tool chain, there is no standard procedure to load an `.elf` file (Step 8 in the development flow). The process depends on the device, memory configuration, prototyping board, and software development platform. We need to consult the specific manual or user guide to complete this task.

8.5.2 MMIO subsystem

Since the MMIO subsystem's controller and the attached IP cores are constructed from scratch and use no vendor's proprietary IPs or components, the HDL codes are completely portable. They can be implemented as long as a prototyping board has adequate external peripherals. The only exception is the Artix's built-in ADC (analog to digital converter), known as *XADC*, which is only available for newer Xilinx devices.

Since the Nexys 4 DDR board contains all the needed peripherals, all MMIO IP cores can be implemented and tested without any external component. Some peripherals may not be available on other prototyping boards. However, the external circuitries are quite simple and can be easily implemented on a breadboard. The schematics for these peripherals can be found in the Nexys 4 DDR on-line manual and reconstructed accordingly.

8.5.3 Video subsystem

While the majority of the video subsystem is designed from scratch, three components – clock management circuit, line buffer, and frame buffer – utilize vendor's proprietary IP cores. The clock management circuit and line buffer accommodate the VGA synchronization, whose clock rate is different from system clock rate. The former requires a PLL (phase-locked loop) like macro cell and the latter is based on a dual-clock FIFO buffer macro cell. Although these macro cells are proprietary, they are common and can be found in all FPGA devices. The proper macro cells can be instantiated in HDL code directly. Thus, the clock management circuit and line buffer do not lead to serious portability issues.

The frame buffer tends to be the most troublesome and least portable IP core in the FPro framework. The key part of the frame buffer is a dual-port memory that is

accessed by the processor and frame control. The latter retrieves data from memory and converts the data into a video stream. The buffer requires a substantial amount of RAM and thus should be implemented by external memory devices. This raises several issues:

- FPGA prototyping boards have different types of memory devices and configurations and some simpler boards may have none.
- Except for simple SRAM devices, a sophisticated proprietary memory controller IP core is needed.
- The frame buffer control must interface with the proprietary memory controller and implement the dual-port access control circuit.
- The same external memory device may be used as processor's RAM and frame buffer at the same time. The partition further complicates the interface and configuration.

Thus, it is difficult to construct a portable frame buffer.

To demonstrate the design principle, the book uses FPGA's internal memory for the video memory. 350 KB of internal RAM is allocated for a frame buffer with a 9-bit VGA resolution. This is doable because the Nexys 4 DDR board contain a large XC7A100T device. It cannot be duplicated in boards with smaller devices. One possible alternative is to reduce the color depth from 9 bits to 1 bit.

Some advanced prototyping boards use HDMI port for the video output. Instead of using a DAC to generate the analog signal, the HDMI interface encodes the output from the line buffer, "serializes" the data, and transmits the video signal digitally through three serial lines. Thus, additional circuits must be added to accommodate the new interface.

8.6 ORGANIZATION

The remaining book consists of three parts. The rest of Part II provides an overview of the hardware architecture and the bare metal embedded software development via the construction of the *vanilla FPro system*, which contains a timer core, a UART core, a GPI (general-purpose input) core, and a GPO (general-purpose output) core. The conceptual diagram is shown in Figure 8.5.

Part III shows how to design an array of MMIO cores for the peripherals on the Nexys 4 DDR prototyping board, including a PWM (pulse width modulation) core, a debouncing core, a seven-segment LED core, a Xilinx XADC controller core, an SPI core, an I^2C core, a PS2 core, and a music synthesis module with a DDFS (direct digital frequency synthesis) core and an ADSR (attack-decay-sustain-release) envelope core. Part IV discusses the video subsystem framework and covers construction of relevant IP cores.

8.7 BIBLIOGRAPHIC NOTES

Embedded systems encompass a spectrum of design issues. The two books, *Embedded System Design: A Unified Hardware/Software Introduction* by F. Vahid and T. D. Givargis and *Computers as Components: Principles of Embedded Computing System Design, 2nd edition,* by W. Wolf, provide a comprehensive discussion. Software-hardware co-design is an emerging research area. *A Practical Introduction*

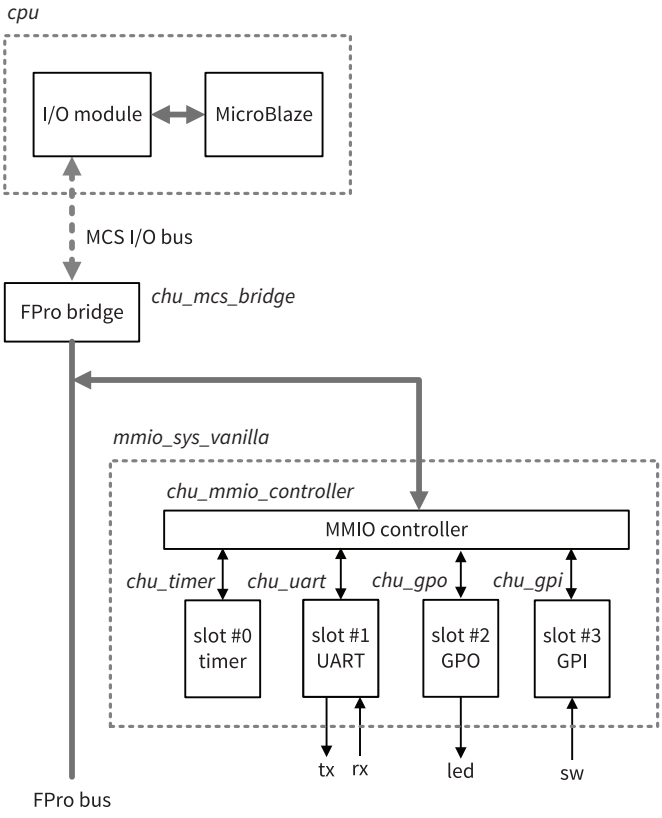

Figure 8.5 Vanilla FPro system.

to Hardware/Software Codesign by P. R. Schaumont addresses the basic concepts and issues of combining hardware and software into a single system.

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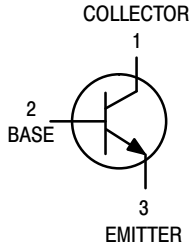


MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Value	Unit
Collector − Emitter Voltage	V_{CEO}	40	Vdc
Collector − Base Voltage	V_{CBO}	75	Vdc
Emitter − Base Voltage	V_{EBO}	6.0	Vdc
Collector Current − Continuous	I_C	600	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

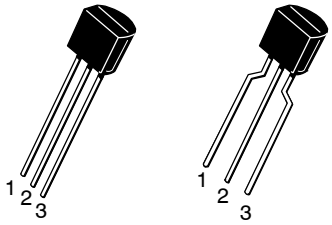
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W

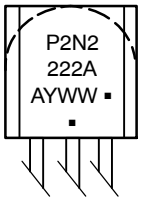
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

TO−92
CASE 29
STYLE 17



MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
P2N2222AG	TO−92 (Pb−Free)	5000 Units/Bulk
P2N2222ARL1G	TO−92 (Pb−Free)	2000/Tape & Ammo

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector – Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	$V_{(BR)CEO}$	40	–	Vdc
Collector – Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	$V_{(BR)CBO}$	75	–	Vdc
Emitter – Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	$V_{(BR)EBO}$	6.0	–	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 3.0 Vdc)	I_{CEX}	–	10	nAdc
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0, T_A = 150°C)	I_{CBO}	– –	0.01 10	μAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)	I_{EBO}	–	10	nAdc
Collector Cutoff Current (V_{CE} = 10 V)	I_{CEO}	–	10	nAdc
Base Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 3.0 Vdc)	I_{BEX}	–	20	nAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 0.1 mAdc, V_{CE} = 10 Vdc) (I_C = 1.0 mAdc, V_{CE} = 10 Vdc) (I_C = 10 mAdc, V_{CE} = 10 Vdc) (I_C = 10 mAdc, V_{CE} = 10 Vdc, T_A = −55°C) (I_C = 150 mAdc, V_{CE} = 10 Vdc) (Note 1) (I_C = 150 mAdc, V_{CE} = 1.0 Vdc) (Note 1) (I_C = 500 mAdc, V_{CE} = 10 Vdc) (Note 1)	h_{FE}	 35 50 75 35 100 50 40	 – – – – 300 – –	–
Collector – Emitter Saturation Voltage (Note 1) (I_C = 150 mAdc, I_B = 15 mAdc) (I_C = 500 mAdc, I_B = 50 mAdc)	$V_{CE(sat)}$	 – –	 0.3 1.0	Vdc
Base – Emitter Saturation Voltage (Note 1) (I_C = 150 mAdc, I_B = 15 mAdc) (I_C = 500 mAdc, I_B = 50 mAdc)	$V_{BE(sat)}$	 0.6 –	 1.2 2.0	Vdc
SMALL–SIGNAL CHARACTERISTICS				
Current – Gain – Bandwidth Product (Note 2) (I_C = 20 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)C	f_T	300	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{obo}	–	8.0	pF
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)	C_{ibo}	–	25	pF
Input Impedance (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz) (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{ie}	 2.0 0.25	 8.0 1.25	kΩ
Voltage Feedback Ratio (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz) (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{re}	 – –	 8.0 4.0	X 10^{-4}
Small–Signal Current Gain (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz) (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	 50 75	 300 375	–
Output Admittance (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz) (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{oe}	 5.0 25	 35 200	μMhos
Collector Base Time Constant (I_E = 20 mAdc, V_{CB} = 20 Vdc, f = 31.8 MHz)	$rb'C_c$	–	150	ps
Noise Figure (I_C = 100 μAdc, V_{CE} = 10 Vdc, R_S = 1.0 kΩ, f = 1.0 kHz)	N_F	–	4.0	dB

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
2. f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Max	Unit
SWITCHING CHARACTERISTICS					
Delay Time	(V_{CC} = 30 Vdc, $V_{BE(off)}$ = −2.0 Vdc, I_C = 150 mAdc, I_{B1} = 15 mAdc) (Figure 1)	t_d	–	10	ns
Rise Time		t_r	–	25	ns
Storage Time	(V_{CC} = 30 Vdc, I_C = 150 mAdc, I_{B1} = I_{B2} = 15 mAdc) (Figure 2)	t_s	–	225	ns
Fall Time		t_f	–	60	ns

SWITCHING TIME EQUIVALENT TEST CIRCUITS

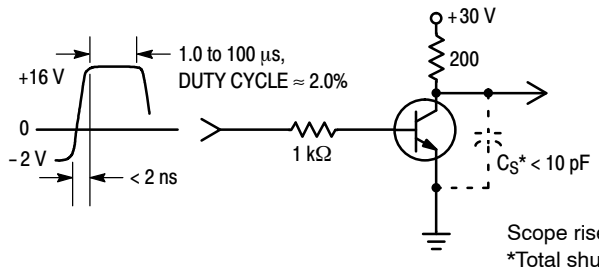
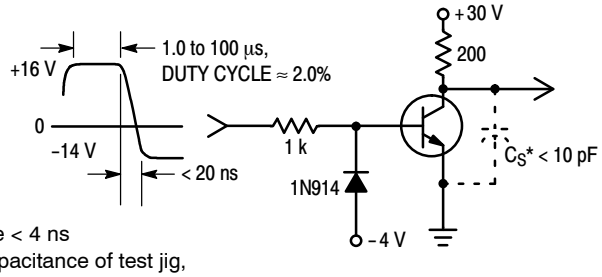


Figure 1. Turn−On Time



Scope rise time < 4 ns
*Total shunt capacitance of test jig, connectors, and oscilloscope.

Figure 2. Turn−Off Time

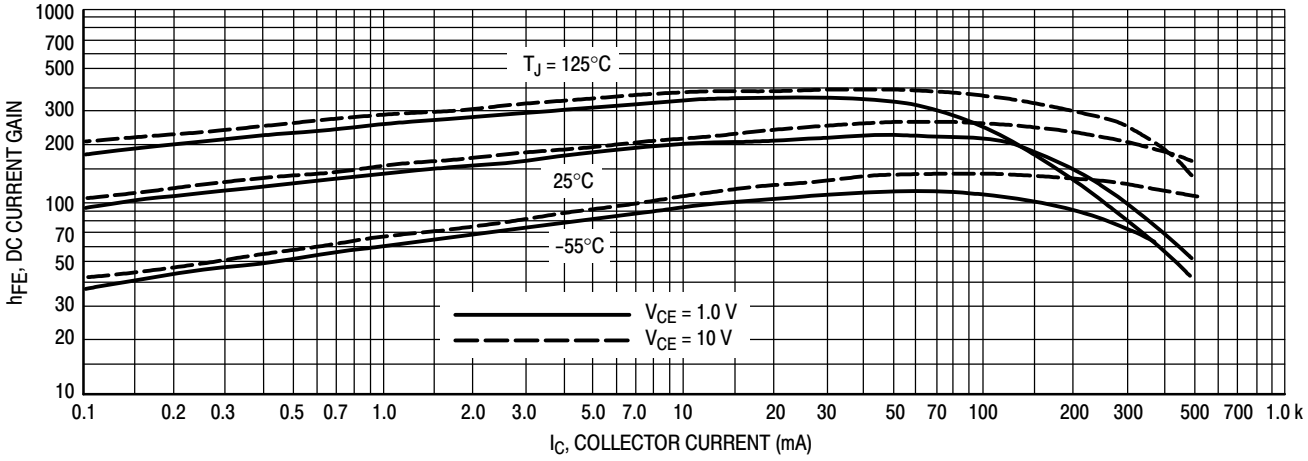


Figure 3. DC Current Gain

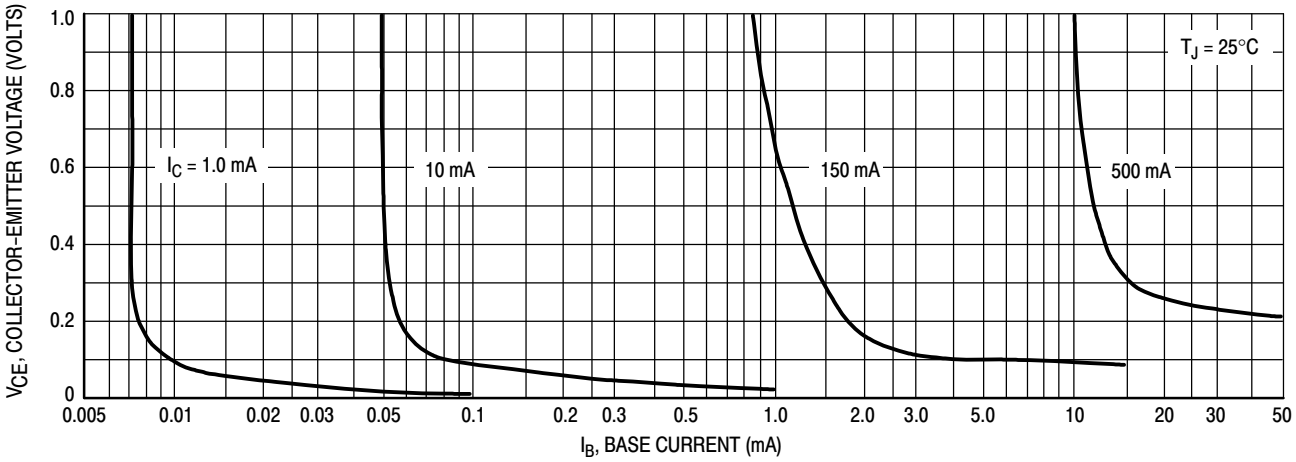


Figure 4. Collector Saturation Region

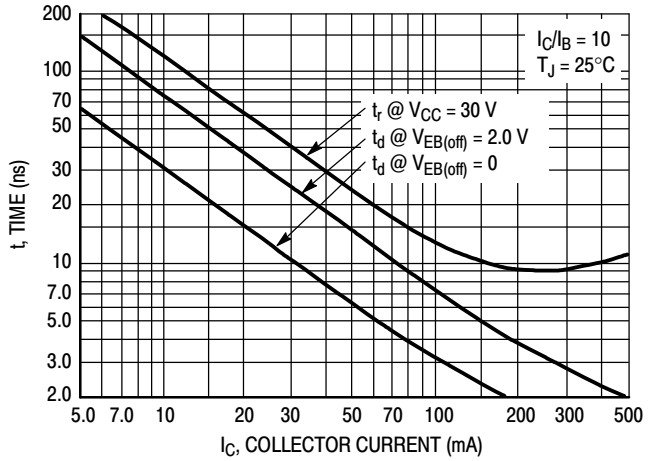


Figure 5. Turn – On Time

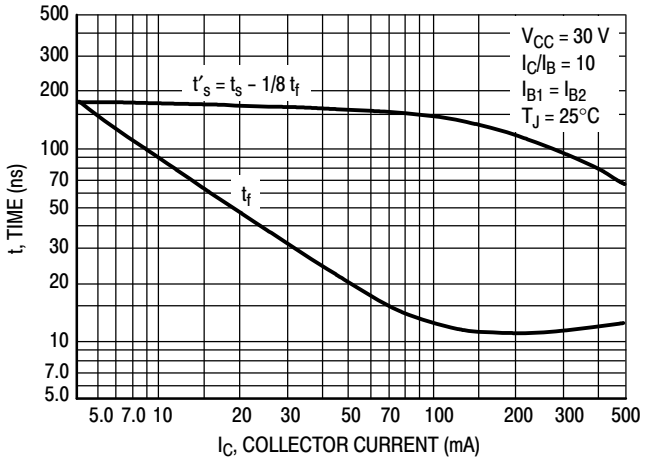


Figure 6. Turn – Off Time

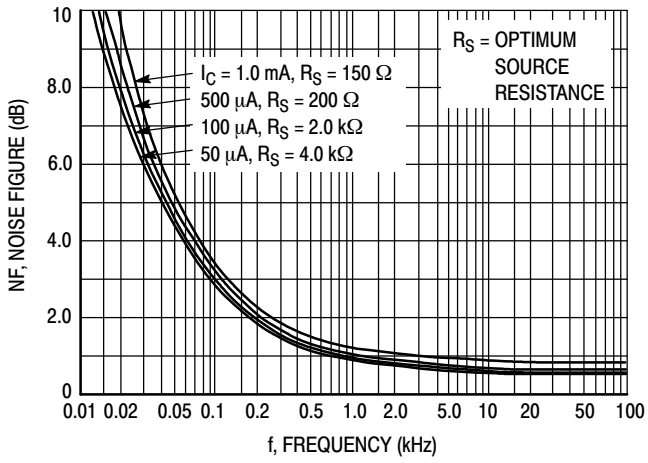


Figure 7. Frequency Effects

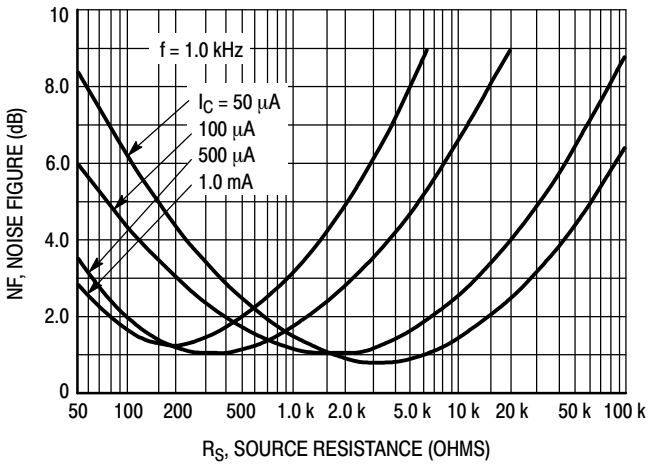


Figure 8. Source Resistance Effects

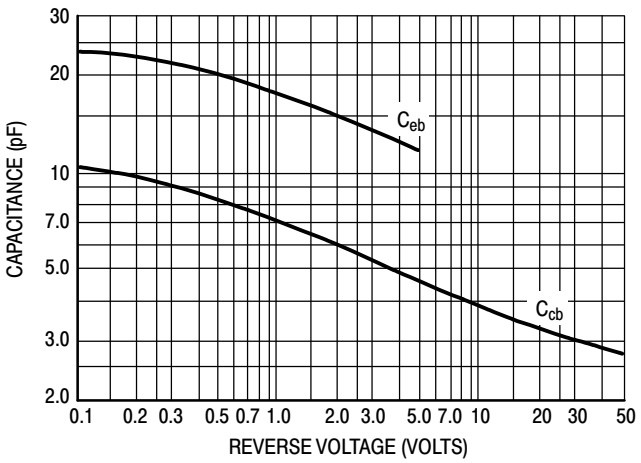


Figure 9. Capacitances

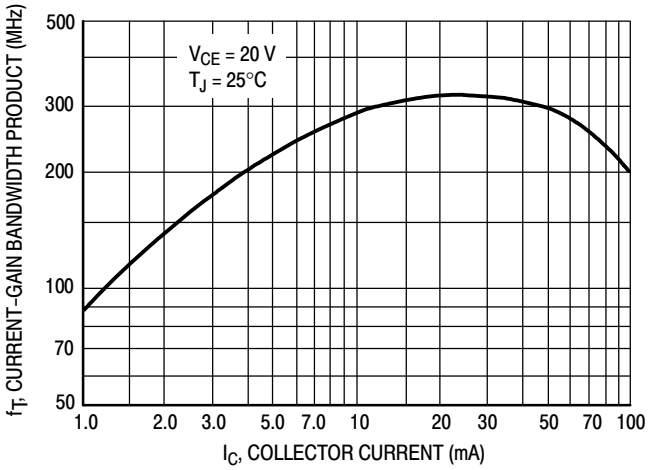


Figure 10. Current−Gain Bandwidth Product

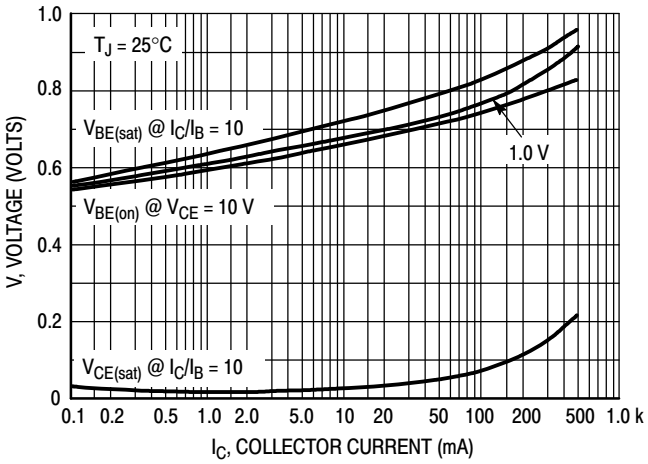


Figure 11. “On” Voltages

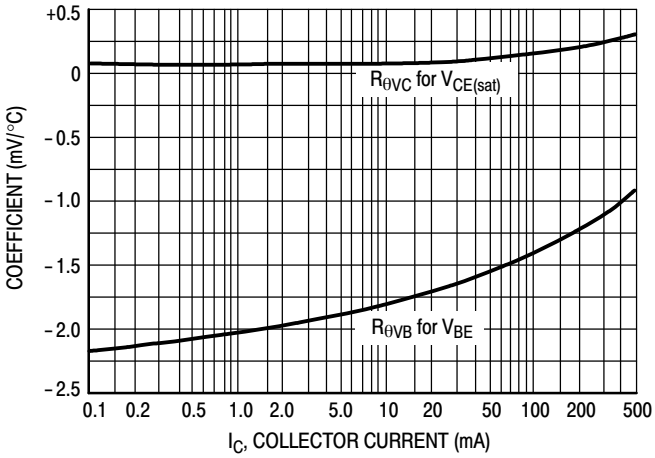
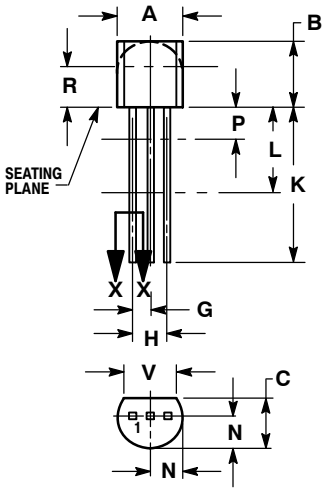


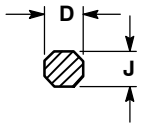
Figure 12. Temperature Coefficients

PACKAGE DIMENSIONS

TO−92 (TO−226)
CASE 29−11
ISSUE AM



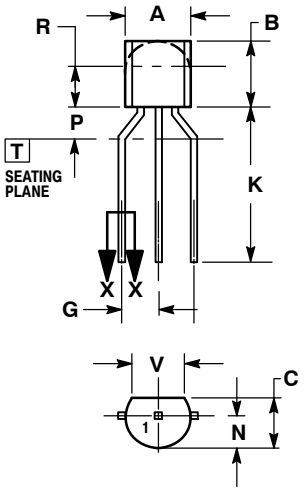
STRAIGHT LEAD
BULK PACK



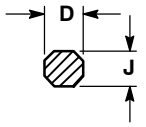
SECTION X−X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---



BENT LEAD
TAPE & REEL
AMMO PACK



SECTION X−X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	MILLIMETERS	
DIM	MIN	MAX
A	4.45	5.20
B	4.32	5.33
C	3.18	4.19
D	0.40	0.54
G	2.40	2.80
J	0.39	0.50
K	12.70	---
N	2.04	2.66
P	1.50	4.00
R	2.93	---
V	3.43	---

STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

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UNIVERSIDAD PRIVADA DE TACNA

FACULTAD DE INGENIERIA

ESCUELA PROFESIONAL DE INGENIERIA ELECTRÓNICA

“PERFIL DE UN INVERNADERO PARA EL FUNDO DE LA UPT”

Presentado por:

Cándido Molanes Miovich

Código : 2012042251

Tacna- Perú

2018

Perfil del proyecto

1. **Introducción**

2. **Diagnóstico y descripción del problema que se desea enfrentar** (1 página)

Retrocedamos 20 años en el tiempo, la zona de agricultura en Tacna ocupaba una fracción del valle del rio Caplina. Actualmente en el año 2018, los terrenos de cultivo van expandiéndose cada vez más, se extienden hasta llegar a terrenos cercanos al litoral. Los mayores problemas que se presentan son la escasez de agua por los cambios climáticos y el uso deficiente del recurso hídrico, por el uso de métodos precarios (riego por surcos, inundación). Un agricultor está acostumbrado a regar y fertilizar manualmente 3 veces a la semana sus plantas, lo que termina en un desperdicio de agua y fertilizantes.

Pocos propietarios de estas tierras usan invernaderos, los cuales empelan dos métodos distintos: como viveros, para cultivar todo tipo de plantas hasta que alcanzan el estado adecuado para su trasplante, distribución y venta (etapa de semilla a plantín), con un uso de todo el año, y como invernadero para cultivar algunos tipos de plantas hasta alcanzar una producción determinada (etapa de semilla a fruto), con un uso de 9 meses, ya que los 3 meses de verano prefiere cultivar en el exterior, por el costo elevado de bajar la temperatura, lo cual está comprobado hasta el momento que no es rentable utilizar un control de temperatura. Cabe resaltar que es vital monitorear la temperatura y humedad ambiental por el problema de garuas esporádicas durante el año.

Ambos métodos de cultivo interno e externo tienen una tecnología de riego, que está muy limitada a un programador de riego de alto costo el cual es programado por un ingeniero agrónomo para regar en determinados horarios. Dependiendo de la evaporación, temperatura promedio, vientos, etc. Extraen mediante estadística cuantos minutos deben regar el cultivo, lo cual no tiene el rendimiento óptimo.

Tomando en cuenta estas consideraciones en conjunto a la falta de capacitación de los agricultores han logrado una baja productividad no solo de tomate sino de otros productos agrícolas en la ciudad, sobre todo esto se ve en la época de invierno, en la cual algunos propietarios no son capaces de producir y otros no logran cubrir la demanda de exportación.

Las condiciones meteorológicas están en constante cambio, afectando la agricultura en Tacna y el mundo. Sin medidas prioritarias, muchas personas están en riesgo de padecer hambre, nuevas formas de cultivar son más necesarias que nunca.

3. Resumen (propuesta)

Antes de empezar con la propuesta se hicieron preguntas a un experto con más de 15 años de experiencia en invernaderos en Tacna.

¿Qué tipo de perfil externo de invernadero se utiliza en la ciudad de Tacna?

Se utiliza un invernadero tipo capilla a dos aguas con una malla antiáfida, no hay discusión de querer poner uno de plástico o vidrio.

¿Cuáles son los parámetros más importantes y dentro de que rango se deben manejar en Tacna?

El parámetro más importante es la humedad del suelo de las plantas. Los parámetros de temperatura, humedad ambiental se usa como referencia para calcular aproximadamente cuanto va a consumir de agua la planta y para resolver cualquier inconveniente temporal de lluvias esporádicas.

Variable	**Definición conceptual**	**Indicadores**
Temperatura (Monitorear)	Grado o nivel térmico del invernadero Grado o nivel	13-30ºC
Humedad relativa (Monitorear)	Cantidad de agua en el aire del invernadero en forma de vapor	60-80%
Humedad del suelo (Monitorear y controlar	Cantidad de agua por volumen de tierra que hay en el cultivo	20-25 (VWC) (Dependiendo altura de la base de la planta)

¿En qué momento se activa el riego, se debería regar las 24 horas del día?

Normalmente las plantas se alimentan de 6am - 6pm, y durante ese lapso de tiempo se debe activar las veces que necesite la planta alimentarse, el actuador debe fertirrigar cuantas veces lo necesite.

En consecuencia, ante lo mencionado anteriormente se propone:

- Mezclar el agua y fertilizantes en un tanque, para luego suministrarlo a la planta en base a un sensor que nos indique si necesita o no agua.

- Monitorear la temperatura y humedad ambiental del invernadero mediante un solo sensor que mide ambos parámetros.

A continuación, se muestra el flujo que habrá en el invernadero.

Fig. 1. "Diagrama conceptual de la producción en invernadero."

Monitoreo de temperatura

Una planta de tomate no soporta el frio ni tampoco el calor, por lo que las temperaturas por debajo de 10ºC y por encima de 35ºC impedirán y reducirán el desarrollo de frutos.

La planta de tomate tiene un crecimiento normal y un buen desarrollo de frutos cuando su clima es cálido con una temperatura diurna de 21-29,5ºC y una nocturna de 18,5-21ºC

Monitoreo de humedad ambiental

La cantidad de vapor de agua en el aire del interior del invernadero es medida en porcentaje por la humedad relativa, esta no es una variable climática que influya directamente al crecimiento del cultivo, aunque su control es de peculiar interés. Pero

para evitar la aparición y desarrollo de enfermedades fúngicas es necesario que la humedad relativa se mantenga entre 60 y 80%.

Sensor propuesto para temperatura y humedad

Pmod HYGRO: Sensor de temperatura y humedad digital

Costo: s/55

Control de humedad del suelo

La medición de humedad del suelo se basa en la medición de contenido volumétrico de agua (vwc) o potencial matricial del suelo. Para fijar un control sobre la humedad del suelo, debemos determinar el contenido de humedad.

Sensor propuesto

Watermark 200ss

Costo: s/300

Actuador propuesto

Electrovalvula Burket ½’

Costo : S/300 soles

Controlador propuesto

FPGA nexys 4

Costo: Gratis en la escuela se cuenta con 4

4. Descripción general (Invernadero en el fundo dimensiones del invernadero amalsicos.

Se implementará 1 invernadero tipo capilla a dos aguas para el cultivo de almácigos con un sistema de aspersión, previsto para suministrar el agua y fertilizantes en toda la superficie en 4 turnos, con 2 electroválvulas en campo, de acuerdo a la lectura de un sensor de humedad de suelo. Se contará con un sensor de monitoreo de temperatura y humedad ambiental. Todo esto tiene un soporte de decisiones quien se encarga de controlar y regular la fertirigación.

Esctructura

Las medidas son:

Ancho: 7m

Largo: 15m

5. Presupuesto Pino S.A.C. (Sistema de riego) y IMATEC(Estructura y malla)

COTIZACION N°. CT1-162068

SEÑORES: UNIVERSIDAD PRIVADA DE TACNA
FECHA : 02/10/2018
REF:
ATENCION:

Es grato el dirigirnos a ustedes con la finalidad de alcanzarles nuestra cotización por lo siguiente:

	CODIGO	DESCRIPCION	CANT.	UND.	V. VENTA S/	VALOR TOTAL S/
1		plantinera			0.00	0.00
2	208500104	ELECTROBOMBA CONFORTO 1 HP INOX 220V-60Hz // NPXM100GIR	1	u.	920.00	920.00
3	121200300	TERMINAL MIXTO MACHO PVC 32 X 40 X 1"	10	u.	2.00	20.00
4	106100800	CODO 90º PE 32 MM	2	u.	4.00	8.00
5	110200300	FILTRO 1" DISCO 130 MIC ROSCADO AZUD	1	u.	75.00	75.00
6	114000400	MANGUITO PVC MIXTO 32 X 1"	3	u.	5.00	15.00
7	1011094	VALVULA ENLACE R/HEMBRA 1"	4	u.	35.00	140.00
8	222500111	TUBO HID PVC 32 MM C-10	4	Tb.	48.00	192.00
9	109501100	ENLACE R/H PE 32 X 1	3	u.	3.00	9.00
10	206200111	CODO 90º PVC SOLDABLE 32MM	9	u.	4.00	36.00
11	221000111	TEE SOLDABLE 32MM	2	u.	9.00	18.00
12	120400800	TAPON FINAL PE 32 MM	2	u.	4.00	8.00
13	109502000	ENLACE R/M PE 20 X 3/4"	3	u.	3.00	9.00
14	118000900	REDUCCION MACHO/HEMBRA PE 1" X 3/4"	3	u.	2.00	6.00
15	213500209	MANGUERA CIEGA 20MM X 1.30 ESP X 300 MTS	0.50	rol	245.00	122.50
16	115100500	NEBULIZADOR GREEN MIST 30 LPH AZUL	100	u.	12.00	1,200.00
17	120400600	TAPON FINAL PE 20MM	3	u.	2.00	6.00
18	115700700	PEGAMENTO PVC 1/4 WELDALL	1	u.	33.00	33.00
19	205600201	CINTA TEFLON 19MM 50MTS	1	u.	20.00	20.00
20		tablerro electrico de proteccion	1	u.	850.00	850.00
21	207800109	DEPOSITO P.E NEGRO X 1500 LTS.	1	u.	1,800.00	1,800.00
22	115500100	PASAMUROS PVC 1"	1	u.	95.00	95.00
23	114000400	MANGUITO PVC MIXTO 32 X 1"	3	u.	5.00	15.00

CONDICIONES DE VENTA:
Forma de Pago : CONTADO
Validez de la Oferta : 0 dias
Lugar de Entrega :

* Los precios unitarios Incluyen IGV

Valor Venta	**S/**	**4,743.63**
IGV 18%	**S/**	**853.85**
Precio de Venta	**S/**	**5,597.48**

CUENTA CORRIENTE

540-1787227-0-41 SOLES BCP-Tacna
540-1773486-1-53 DOLARES BCP - Tacna

0011-0232-01-00072868 SOLES BBVA - Tacna
0011-0232-01-00072876 DOLARES BBVA - Tacna

000-7683944 SOLES SCOTIABANK - TACNA
000-3574714 DOLARES SCOTIABANK - TACNA

0151-072070 DETRACCIONES BCO. DE LA NACION

NAANDANJAIN
A JAIN IRRIGATION COMPANY

GREEN MIST

Super LPD

Boquilla Green Mist

Emisor de doble propósito para nebulizar y regar sobre mesas de propagación

CARACTERÍSTICAS PRINCIPALES

- Gran uniformidad de cobertura
- Tamaño ideal de gotitas para optimizar la dispersión de la fina neblina
- Ausencia de goteo durante el funcionamiento
- Distribución simétrica del riego y sin discontinuidad (sin deflexión y sin zonas “muertas”)
- Elemento antidrenante (LPD) para un perfecto funcionamiento en pulsos
- Bajo costo

CARACTERÍSTICAS TÉCNICAS

- Presión: 2.0 a 3.5 bar
- Caudal: 30 - 40 l/h (ver tabla)
- Requisitos de filtrado: 120 mesh (130 micrones)
- Diámetro de humedecimiento: 1.2 m

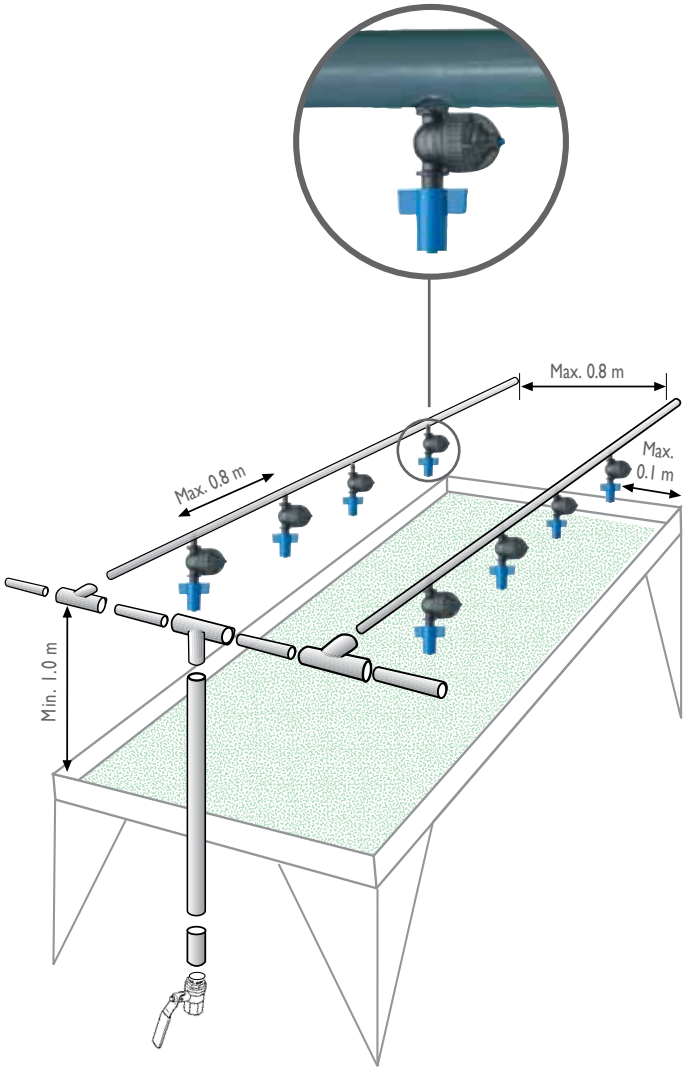
INSTRUCCIONES DE INSTALACIÓN

- Altura de las unidades por encima de las mesas: 1.0 - 1.2 m
- Espaciamiento máximo entre unidades sobre el lateral: 0.8 m
- Espaciamiento máximo entre laterales: 0.8 m
- Distancia máxima del lateral desde el borde del banco: 0.1 m

CAUDALES Y PRESIONES

Presión (bar)	2.0	2.5	3.0	3.5
Caudal (l/h)	30	34	37	40

Diseño esquemático de una instalación sobre tuberia de PVC



	CRIADO Y LOPEZ PERU SAC	
	TLF: 052-314300 Tacna 056-720078 Ica	www.criadoylopez.com
	TÚNEL KIT IMATEC	
	DEPARTAMENTO COMERCIAL	

CLIENTE:	Universidad Privada de Tacna		
UBICACIÓN OBRA:	Fundo de la UPT		
TLF / E-mail:	electrónica.transmite@gmail.com	**FECHA**	04/10/18

TÚNEL KIT IMATEC

ÍNDICE

1.- CARACTERÍSTICAS TÉCNICAS

2.- ESTRUCTURA Y CUBIERTA

2.1.- ESTRUCTURA

- **Arcos de tubo** de diámetro 40 mm y 1,5 mm de espesor, colocados cada 2 m. Anclados sobre piquetas clavadas directamente al suelo.
- **Tirantes y pendolones** de tubo redondo de 32 mm de diámetro y 1,2 mm de espesor. Se coloca un tirante y pendolón cada arco. El tirante es uno de los elementos más importantes en el correcto arriostramiento del invernadero
- El tirante sirve como **soporte de cultivo**, para ello se ha dotado de un refuerzo vertical, el pendolón, que evita el desplazamiento del plano recto del tirante.
- Altura a la cumbrera 3 m
- Altura al tirante 2 m.

2.2.- SISTEMA DE SUJECIÓN

- **5 Correas longitudinales de** tubo de 32 mm de diámetro y 1,2 mm de espesor. Permiten amarrar los arcos entre sí de manera que trabajan a tracción y contracción para la correcta sujeción de la estructura.

- **5 Refuerzos frontales** de arco a arco en cada extremo completan el arriostramiento del invernadero.
- **Tornillería,** todas las uniones están previstas para facilitar el montaje y desmontaje de sus elementos con la mayor facilidad y fiabilidad. Tornillos y tuercas hexagonales DIN-933 y DIN-934 en calidad comercial 5.6, correspondiendo a las designaciones F-7417, según Norma UNE-36-089-72.Resistencia media a la tracción 55 Kg/mm².

2.3.- PUERTA Y VENTILACIÓN

- **2 Puertas Correderas**, colocadas una en cada frontal de dimensiones 2x2 m. Disponen de un paño fijo que se puede cubrir con plástico o con malla para mejorar la ventilación.

- **2 Ventanas frontales abatibles** de dimensiones 2 x 0,6 m. Colocadas en la media luna del invernadero. Incorporan pestillo para un cierre adecuado.

2.4.– CIMENTACIÓN

La estructura no requiere cimentación, lo que facilita y agiliza el montaje. El plástico enterrado en 2 zanjas paralelas al invernadero y cubierto de tierra sujeta fuertemente la estructura al suelo.

2.5.– CUBIERTA

Material de cubierta **plástico térmico de 800gg** (0,2 mm).

Garantía: 48 meses en el norte de España y 36 en el sur

Termicidad: >al 86%

Trasmisión luminosa global: > 92%

12 líneas de monofilamento sujetas en los extremos mantienen el plástico tenso y evitan la formación de bolsas de agua.

2.6.– CALIDAD DEL ACERO

Todo el acero que se utiliza en los invernaderos IMA como materia prima es de probada calidad y homogeneidad y ha sido seleccionado en las mejores acerías europeas.

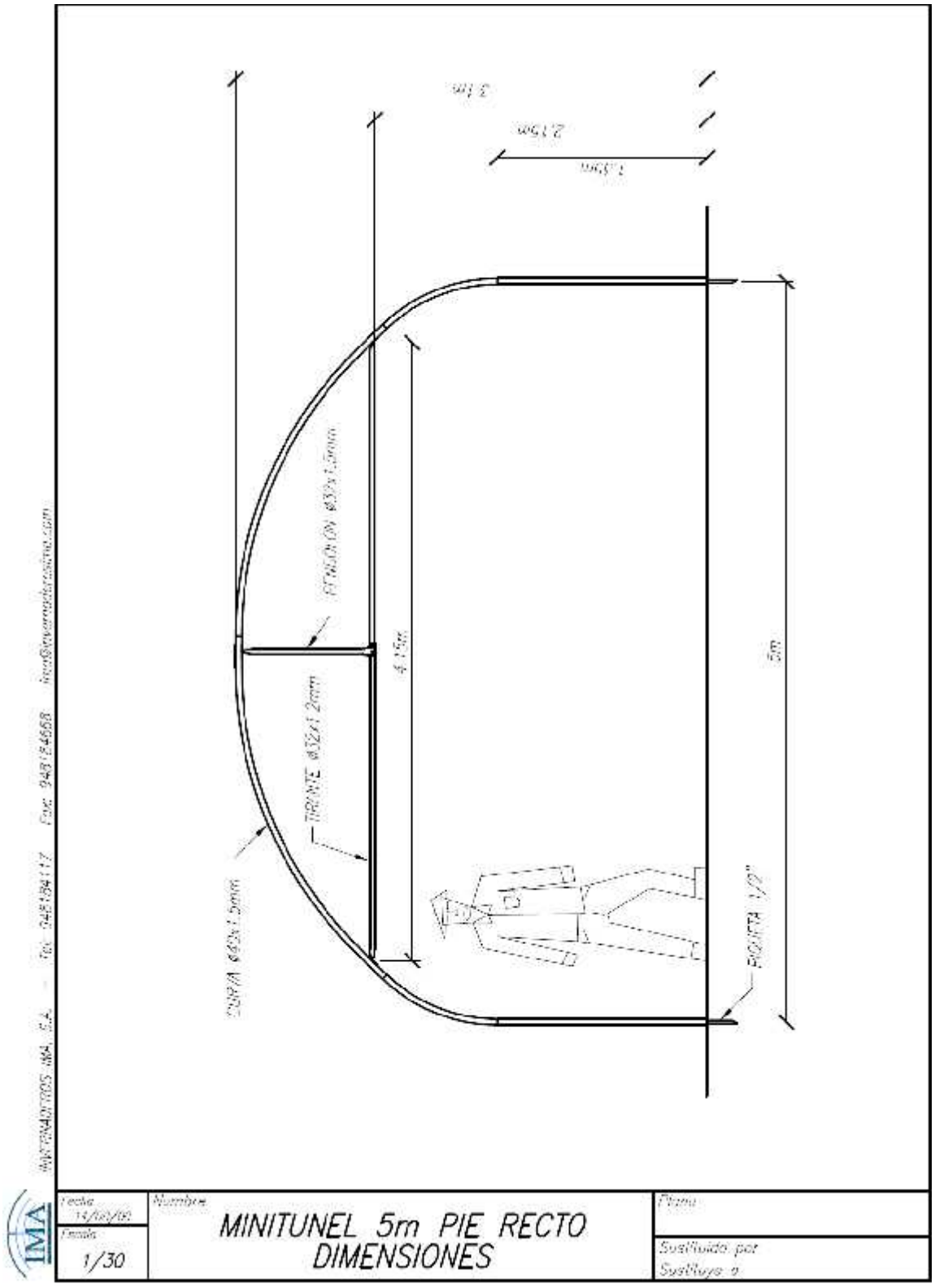
Para la realización de todo tipo de tubos, se parte de fleje comercial, el cual debe poderse plegar, su resistencia máxima no debe pasar de 41-42 Kg/mm². La resistencia media del material empleado es de 35-36 Kg/mm², se puede equiparar con Rst-34.

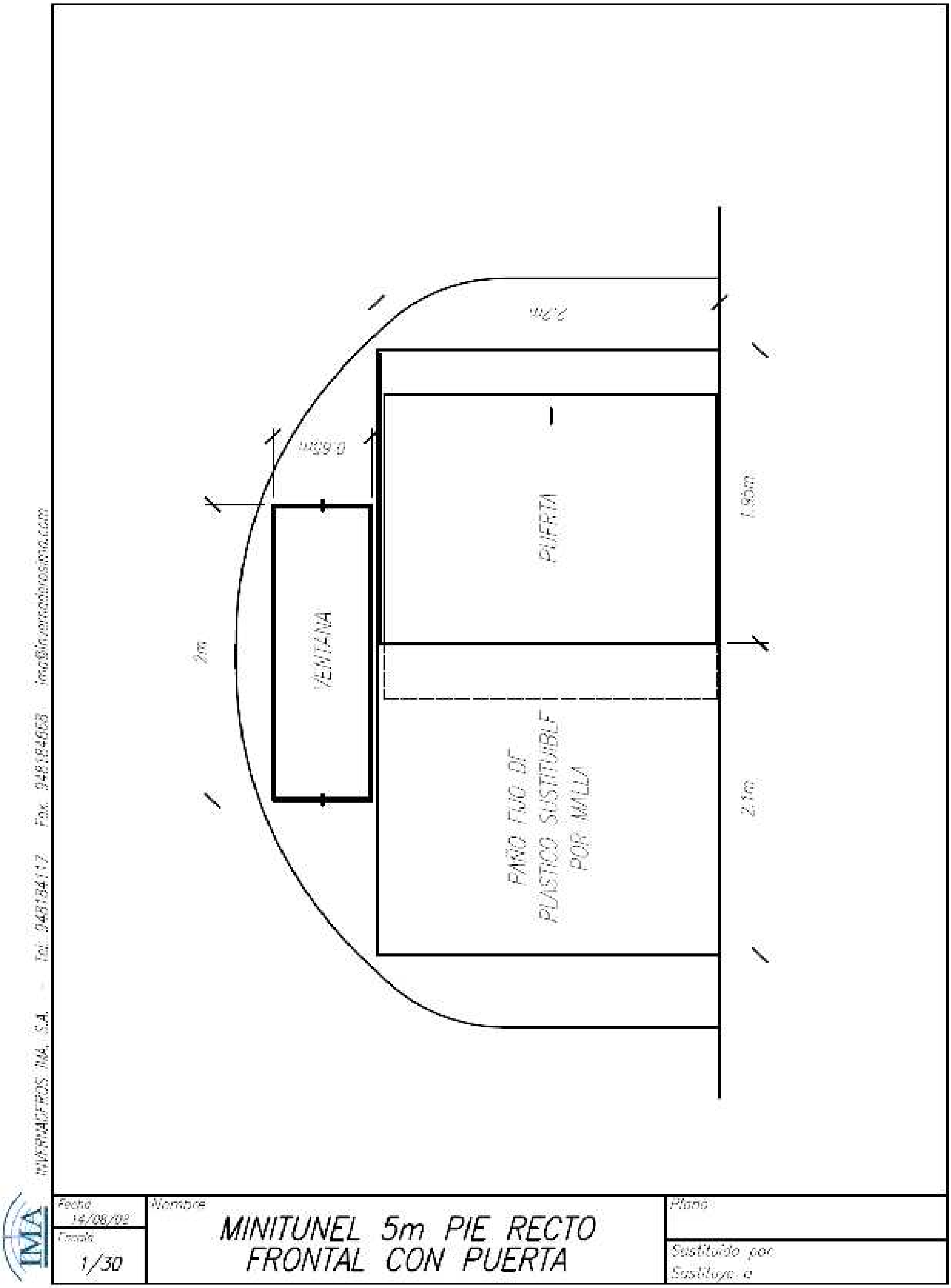
Hay que tener en cuenta que en todo proceso posterior al perfilado para la conformación de los tubos, el material adquiere una resistencia adicional, que mejora sus características, lo cual se ve en los ensayos mecánicos, pero no recogidos en la norma.

2.7.- GALVANIZADO

Todo el material con el que se fabrican los invernaderos IMA, es de Acero galvanizado por Inmersión según el procedimiento Sendzimir. Este proceso consiste en la inmersión en un baño de Zinc a una temperatura específica y constante durante todo el proceso, de chapa de bobina, laminada tanto en frío como en caliente y preparada para el galvanizado con un decapado previo, con lo que se consigue una auténtica fusión entre el acero y el zinc. Este proceso garantiza un recubrimiento de zinc según la norma UNE 36130 y la Euro norma 142-79. Según estas especificaciones el material utilizado es Z-275, con 275 g/m². Con esto se evita cualquier proceso de corrosión.

3.- PLANOS




VENTANA
PUERTA
PAÑO FIJO DE PLASTICO SUSTITUIBLE POR MALLA
2m
2.1m
Fecha 14/06/02
Escala 1/30
Nombre
MINITUNEL 5m PIE RECTO FRONTAL CON PUERTA
Plano
Sustituido por
Sustituye a

4.- FOTOS

Marcaje y piquetas

Ensamblaje arcos, tirantes, pendolones y correas

Estructura

Cubierta plástico

Ventana y Puerta

5.- PRESUPUESTO ESTRUCTURA Y MALLA

El presupuesto es de s/7000.

6. Presupuesto Final

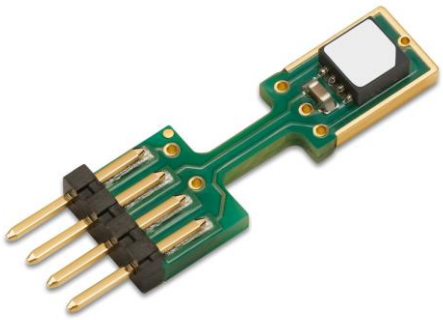
Pino S.A.C. (Sistema de riego) + IMATEC(Estructura y malla) + Tecnología = **s/13 252.48**

SENSIRION
THE SENSOR COMPANY

Datasheet SHT85

Humidity and Temperature Sensor

- High-accuracy RH&T sensor for demanding measurement & test applications
- Typical accuracy of ± 1.5 %RH and ± 0.1 °C
- Pin-type packaging for easy integration and replacement
- Fully calibrated, linearized, and temperature compensated digital output



Product Summary

SHT85 is Sensirion's best-in-class humidity sensor with pin-type connector for easy integration and replacement. It builds on a highly accurate and long-term stable SHT3x sensor that is at the heart of Sensirion's new humidity and temperature platform. The unique package design allows for the best possible thermal coupling to the environment and decoupling from potential heat sources on the main board. The SHT85 features a PTFE membrane dedicated to protect the sensor opening from liquids and dust according to IP67, without affecting the response time of the RH signal. It thus allows for sensor use under harsh environmental conditions, (such as spray water and high exposure to dust). Final accuracy testing on product level ensures best performance, making the SHT85 the ultimate choice for even the most demanding applications.

Benefits of Sensirion's CMOSens® Technology

- High reliability and long-term stability
- Industry-proven technology with a track record of more than 10 years
- Designed for mass production
- Optimized for lowest cost
- Low signal noise

SENSIRION
THE SENSOR COMPANY

Content

1 Humidity and Temperature Sensor Specifications

Relative Humidity

Parameter	Conditions	Value	Units
Accuracy tolerance[1]	Typ.	±1.5	%RH
	Max.	see Figure 1	-
Repeatability[2]	Low, typ.	0.21	%RH
	Medium, typ.	0.15	%RH
	High, typ.	0.08	%RH
Resolution	Typ.	0.01	%RH
Hysteresis	At 25°C	±0.8	%RH
Specified range[3]	Non-condensing environment[4]	0 to 100	%RH
Response time[5]	τ 63%	8[6]	s
Long-term drift[7]	Typ.	<0.25	%RH/y

Table 1: Humidity sensor specifications

Temperature

Parameter	Conditions	Value	Units
Accuracy tolerance[1]	Typ., 20°C to 50 °C	±0.1	°C
	Max.	see Figure 2	-
Repeatability[2]	Low, typ.	0.15	°C
	Medium, typ.	0.08	°C
	High, typ.	0.04	°C
Resolution	Typ.	0.01	°C
Operating range	-	–40 to 105[8]	°C
Response time[9]	τ 63%	>2	s
Long-term drift	Typ.	<0.03	°C/y

Table 2: Temperature sensor specifications

[1] For definition of typ. and max. accuracy tolerance, please refer to the document "Sensirion Humidity Sensor Specification Statement".

[2] The stated repeatability is 3 times the standard deviation (3σ) of multiple consecutive measurement values at constant conditions and is a measure for the noise on the physical sensor output.

[3] Specified range refers to the range for which the humidity sensor specification is guaranteed.

[4] Condensation shall be avoided because of risk of corrosion and leak currents on the PCB. For details about recommended humidity and temperature operating range, please refer to Section 1.2.

[5] Time for achieving 63% of a humidity step function, valid at 25°C and 1 m/s airflow. Humidity response time in the application depends on the design-in of the sensor.

[6] With activated ART function (see Section 4.7) the response time can be improved by a factor of 2.

[7] Typical value for operation in normal RH/T operating range. Max. value is < 0.5 %RH/y. Value may be higher in environments with vaporized solvents, out-gassing tapes, adhesives, packaging materials, etc. For more details please refer to Handling Instructions.

[8] All parts, incl. PCB are rated up to 125°C, except for the connector, which is rated for 105°C.

[9] Temperature response time depends on heat conductivity of sensor substrate and design-in of sensor in application.

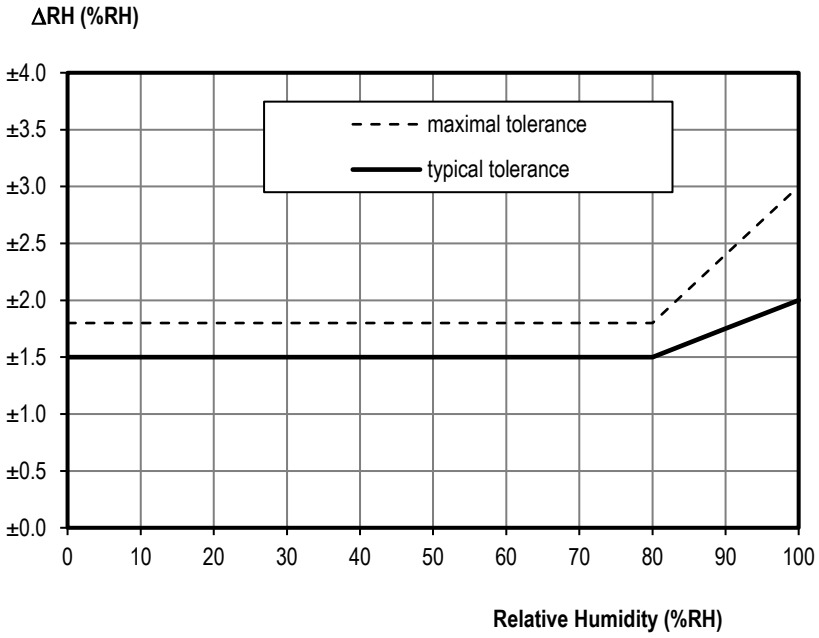


Figure 1: Typical and maximal tolerance for relative humidity in %RH at 25 °C.

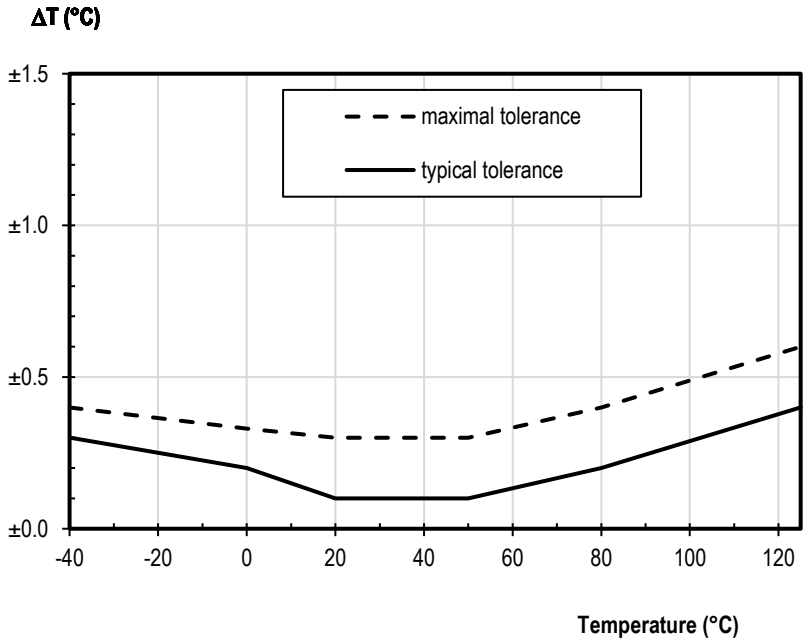


Figure 2: Typical and maximal tolerance for temperature sensor in °C

1.1 RH Accuracy at Various Temperatures

Typical RH accuracy at 25°C is defined in Figure 2. For other temperatures, typical accuracy has been evaluated to be as displayed in Figure 4.

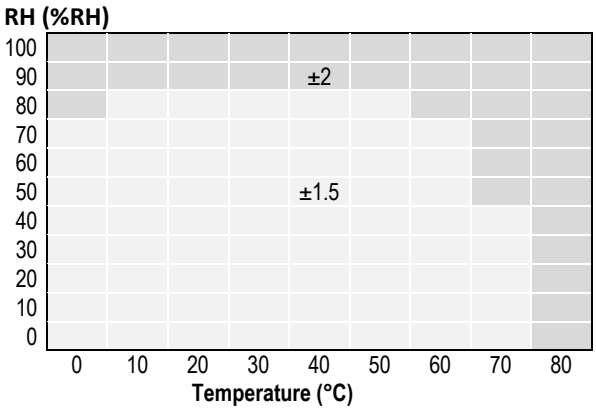


Figure 3: Typical accuracy of relative humidity measurements given in %RH for temperatures 0 – 80°C.

1.2 Recommended Operating Conditions

The sensor shows best performance when operated within recommended normal temperature and humidity range of 5 – 60 °C and 20 – 80 %RH, respectively. Long term exposure to conditions outside normal range, especially at high humidity, may temporarily offset the RH signal (e.g. +3%RH after 60h at >80%RH). After returning into the normal temperature and humidity range, the sensor will slowly come back to calibration state by itself. Prolonged exposure to extreme conditions may accelerate ageing.

To ensure stable operation of the humidity sensor, the conditions described in the document "SHTxx Assembly of SMD Packages", Section "Storage and Handling Instructions" regarding exposure to volatile organic compounds have to be met. Please note as well that this does apply not only to transportation and manufacturing, but also to operation of the SHT85.

2 Electrical Specifications

2.1 Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ.	Max	Units	Comments
Supply voltage	V_{DD}		2.15	3.3	5.5	V	-
Power-up/down level	V_{POR}		1.8	2.1	2.15	V	-
Slew rate change of the supply voltage	$V_{DD,slew}$		-	-	20	V/ms	Voltage changes on the VDD line between $V_{DD,min}$ and $V_{DD,max}$ should be slower than the maximum slew rate; faster slew rates may lead to reset;
Supply current	I_{DD}	Idle state (single shot mode) T= 25°C	-	0.2	12.0	µA	Current when sensor is not performing a measurement during single shot mode
		Idle state (single shot mode) T= 125°C	-	-	6.0		
		Idle state (periodic data acquisition mode)	-	45	-	µA	Current when sensor is not performing a measurement during periodic data acquisition mode
		Measurement	-	600	1500	µA	Average current consumption while sensor is measuring[10]
		Average	-	1.7	-	µA	Average current consumption (continuous operation with one measurement per second)[10]
Heater Power	P_{Heater}	Heater running	3.6	-	33	mW	Depending on the supply voltage

Table 3: Electrical specifications, typical values are valid for T=25°C, min. & max. values for T=-40°C … 125°C.

2.2 Timing Specifications

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
Power-up time	t_{PU}	After hard reset, $V_{DD} \geq V_{POR}$	-	0.5	1.5	ms	Time between V_{DD} reaching V_{PU} and sensor entering idle state
Soft reset time	t_{SR}	After soft reset.	-	0.5	1.5	ms	Time between ACK of soft reset command and sensor entering idle state
Measurement duration	$t_{MEAS,l}$	Low repeatability	-	2.5	4.5	ms	The three repeatability modes differ with respect to measurement duration, noise level and energy consumption.
	$t_{MEAS,m}$	Medium repeatability	-	4.5	6.5	ms	
	$t_{MEAS,h}$	High repeatability	-	12.5	15.5	ms	

Table 4: System timing specifications, valid from -40 °C to 125 °C and VDDmin to VDDmax.

[10] These values can be reduced by using the low power measurement mode, see separate application note.

2.3 Absolute Minimum and Maximum Ratings

Stress levels beyond those listed in Table 5 may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions cannot be guaranteed. Exposure to the absolute maximum rating conditions for extended periods may affect the reliability of the device. Ratings are only tested each at a time.

Parameter	Rating
Supply voltage, V_{DD}	-0.3 to 6 V
Max voltage on pins (pin 1 (SCL); pin 4 (SDA);	-0.3 to VDD+0. V
Input current on any pin	±100 mA
Operating temperature range	-40 to 105 °C
Storage temperature range[11]	-40 to 105 °C
ESD HBM (human body model)[12]	4 kV
ESD CDM (charge device model)[13]	750 V

Table 5: Absolute maximum ratings.

[11] The recommended storage temperature range is 10-50°C. Please consult the document "SHTxx Handling Instructions" for more information.

[12] According to ANSI/ESDA/JEDEC JS-001-2014; AEC-Q100-002.

[13] According to ANSI/ESD S5.3.1-2009; AEC-Q100-011.

3 Pin Assignment

The SHT85 comes with a 4-pin-type connector, see Table 6.

Pin	Name	Comments
1	SCL	Serial clock; input only
2	VDD	Supply voltage; input
3	VSS	Ground
4	SDA	Serial data; input / output

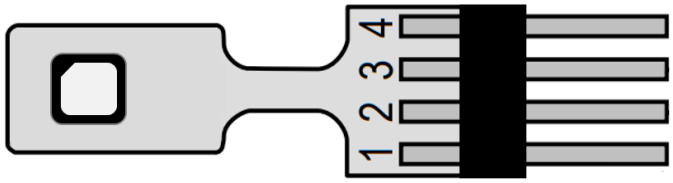


Table 6: SHT85 pin assignment (transparent top view). The die pad is internally connected to VSS.

3.1 Power Pins (VDD, VSS)

The electrical specifications of the SHT85 are shown in Table 3. Decoupling of VDD and VSS by a 100nF capacitor is integrated on the front side of the sensor packaging. See Figure 4 for a typical application circuit.

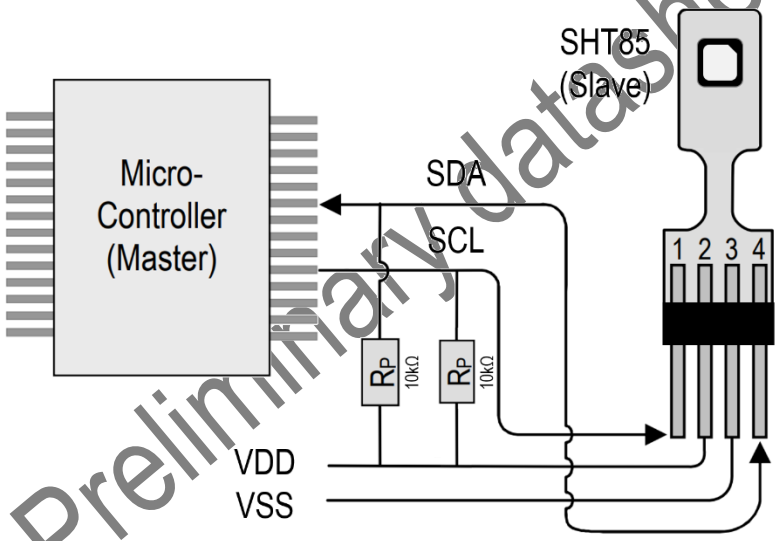


Figure 4: Typical application circuit

3.2 Serial Clock and Serial Data (SCL, SDA)

SCL is used to synchronize the communication between microcontroller and the sensor. The clock frequency can be freely chosen between 0 to 1000 kHz.

The SDA pin is used to transfer data to and from the sensor. Communication with frequencies up to 400 kHz must meet the I2C *Fast Mode*[14] standard. Communication frequencies up to 1 Mhz are supported following the specifications given in Table 19.

[14] http://www.nxp.com/documents/user_manual/UM10204.pdf

4 Operation and Communication

The SHT85 supports I2C fast mode (and frequencies up to 1000 kHz). For detailed information on the I2C protocol, refer to NXP I2C-bus specification[15].

After sending a command to the sensor a minimal waiting time of 1ms is needed before another command can be received by the sensor.

Furthermore, to keep self-heating below 0.1°C, SHT85 should not be active for more than 10% of the time.

All SHT85 commands and data are mapped to a 16-bit address space. Additionally, data and commands are protected with a CRC checksum. This increases communication reliability. The 16 bits commands to the sensor already include a 3 bit CRC checksum. Data sent from and received by the sensor is always succeeded by an 8 bit CRC.

In write direction it is mandatory to transmit the checksum, since the SHT85 only accepts data if it is followed by the correct checksum. In read direction it is left to the master to read and process the checksum.

4.1 Power-Up and Communication Start

The sensor starts powering-up after reaching the power-up threshold voltage V_{POR} specified in Table 3. After reaching this threshold voltage the sensor needs the time t_{PU} to enter idle state. Once the idle state is entered it is ready to receive commands from the master (microcontroller).

Each transmission sequence begins with a START condition (S) and ends with a STOP condition (P) as described in the I2C-bus specification. Whenever the sensor is powered up, but not performing a measurement or communicating, it automatically enters idle state for energy saving. This idle state cannot be controlled by the user.

4.2 Starting a Measurement

A measurement communication sequence consists of a START condition, the I2C write header (7-bit I2C device address plus 0 as the write bit) and a 16-bit measurement command. The proper reception of each byte is indicated by the sensor. It pulls the SDA pin low (ACK bit) after the falling edge of the 8th SCL clock to indicate the reception. A complete measurement cycle is depicted in Table 7.

With the acknowledgement of the measurement command, the SHT85 starts measuring humidity and temperature.

4.3 Measurement Commands for Single Shot Data Acquisition Mode

In this mode one issued measurement command triggers the acquisition of *one data pair*. Each data pair consists of one 16-bit temperature and one 16-bit humidity value (in this order). During transmission each data value is always followed by a CRC checksum, see Section 4.4.

In single shot mode different measurement commands can be selected. The 16-bit commands are shown in Table 7. They differ with respect to repeatability (low, medium and high).

The repeatability setting influences the measurement duration and thus the overall energy consumption of the sensor. This is explained in Section 2.

[15] http://www.nxp.com/documents/user_manual/UM10204.pdf

Condition	Hex. code	
Repeatability	MSB	LSB
High	0x24	00
Medium		0B
Low		16
e.g. 0x2400: high repeatability measurement.		

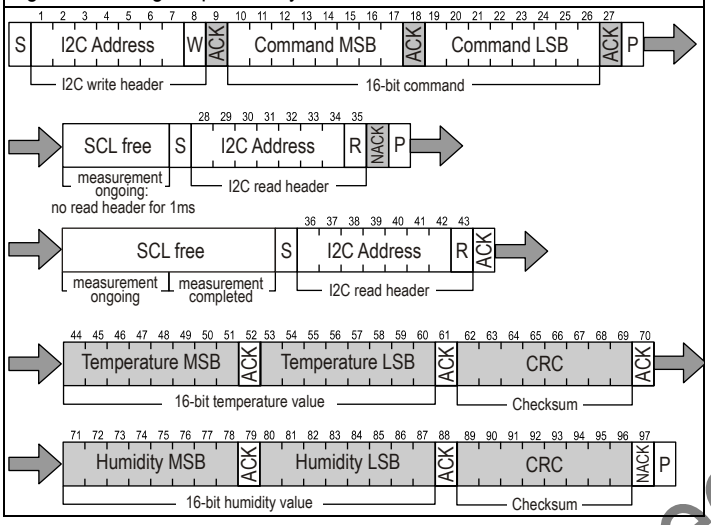


Table 7: Measurement commands in single shot mode. The first "SCL free" block indicates a minimal waiting time of 1ms. (Clear blocks are controlled by the microcontroller, grey blocks by the sensor).

4.4 Readout of Measurement Results for Single Shot Mode

After the sensor has completed the measurement, the master can read the measurement results (pair of RH & T) by sending a START condition followed by an I2C read header.

The sensor responds to a read header with a not acknowledge (NACK), if the measurement is still ongoing and thus no data is present.

If the measurement is completed, the sensor will acknowledge the reception of the read header and send two bytes of data (temperature) followed by one byte CRC checksum and another two bytes of data (relative humidity) followed by one byte CRC checksum. Each byte must be acknowledged by the microcontroller with an ACK condition for the sensor to continue sending data. If the sensor does not receive an ACK from the master after any byte of data, it will not continue sending data.

The sensor will send the temperature value first and then the relative humidity value. After having received the checksum for the humidity value a NACK and stop condition should be sent (see Table 7).

The I2C master can abort the read transfer with a NACK condition after any data byte if it is not interested in subsequent data, e.g. the CRC byte or the second measurement result, in order to save time.

In case the user needs humidity and temperature data but does not want to process CRC data, it is recommended to read the two temperature bytes of data with the CRC byte (without processing the CRC data); after having read the two humidity bytes, the read transfer can be aborted with a with a NACK.

4.5 Measurement Commands for Periodic Data Acquisition Mode

In this mode one issued measurement command yields *a stream of data pairs*. Each data pair consists of one 16-bit temperature and one 16-bit humidity value (in this order).

In periodic mode different measurement commands can be selected. The corresponding 16-bit commands are shown in Table 8. They differ with respect to repeatability (low, medium and high) and data acquisition frequency (0.5, 1, 2, 4 & 10 measurements per second, mps).

The data acquisition frequency and the repeatability setting influences the measurement duration and the current consumption of the sensor. This is explained in Section 2 of this datasheet.

If a measurement command is issued, while the sensor is busy with a measurement (measurement durations see Table 4), it is recommended to issue a break command first (see Section 4.8). Upon reception of the break command the sensor will abort the ongoing measurement and enter the single shot mode.

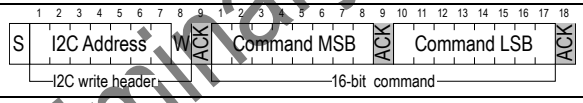
Condition		Hex. code	
Repeatability	mps	MSB	LSB
High	0.5	0x20	32
Medium			24
Low			2F
High	1	0x21	30
Medium			26
Low			2D
High	2	0x22	36
Medium			20
Low			2B
High	4	0x23	34
Medium			22
Low			29
High	10	0x27	37
Medium			21
Low			2A
e.g. 0x2130: 1 high repeatability mps - measurement per second			
			

Table 8: Measurement commands for periodic data acquisition mode (Clear blocks are controlled by the microcontroller, grey blocks by the sensor). N.B.: At the highest mps setting self-heating of the sensor might occur.

4.6 Readout of Measurement Results for Periodic Mode

Transmission of the measurement data can be initiated through the fetch data command shown in Table 9. If no measurement data is present the I2C read header is responded with a NACK (Bit 9 in Table 9) and the communication stops. After the read out command fetch data has been issued, the data memory is cleared, i.e. no measurement data is present.

Command	Hex code
Fetch Data	0x E0 00

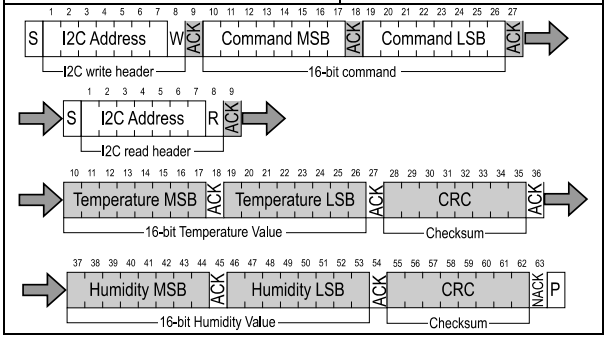


Table 9: Fetch Data command (Clear blocks are controlled by the microcontroller, grey blocks by the sensor).

4.7 ART Command

The ART (accelerated response time) feature can be activated by issuing the command in Table 10. After issuing the ART command the sensor will start acquiring data with a frequency of 4Hz.

The ART command is structurally similar to any other command in Table 8. Hence Section 4.5 applies for starting a measurement, Section 4.6 for reading out data and Section 4.8 for stopping the periodic data acquisition.

Command	Hex Code
Periodic Measurement with ART	0x2B32

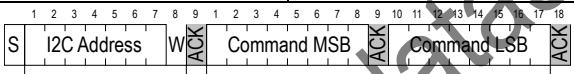


Table 10: Command for a periodic data acquisition with the ART feature (Clear blocks are controlled by the microcontroller, grey blocks by the sensor).

4.8 Break command / Stop Periodic Data Acquisition Mode

The periodic data acquisition mode can be stopped using the break command shown in Table 11. It is recommended to stop the periodic data acquisition prior to sending another command (except Fetch Data command) using the break command. Upon reception of the break command the sensor will abort the ongoing measurement and enter the single shot mode. This takes 1ms.

Command	Hex Code
Break	0x3093

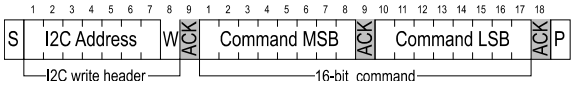


Table 11: Break command (Clear blocks are controlled by the microcontroller, grey blocks by the sensor).

4.9 Reset

A system reset of the SHT85 can be generated externally by issuing a command (soft reset). Additionally, a system reset is generated internally during power-up. During the reset procedure the sensor will not process commands.

Interface Reset

If communication with the device is lost, the following signal sequence will reset the serial interface: While leaving SDA high, toggle SCL nine or more times. This must be followed by a Transmission Start sequence preceding the next command. This sequence resets the interface only. The status register preserves its content.

Soft Reset / Re-Initialization

The SHT85 provides a soft reset mechanism that forces the system into a well-defined state without removing the power supply. When the system is in idle state the soft reset command can be sent to the SHT85. This triggers the sensor to reset its system controller and reloads calibration data from the memory. In order to start the soft reset procedure the command as shown in Table 12 should be sent.

It is worth noting that the sensor reloads calibration data prior to every measurement by default.

Command	Hex Code
Soft Reset	0x30A2

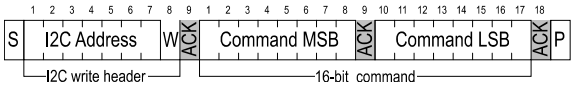


Table 12: Soft reset command (Clear blocks are controlled by the microcontroller, grey blocks by the sensor).

Reset through General Call

Additionally, a reset of the sensor can also be generated using the "general call" mode according to I2C-bus specification[15]. It is important to understand that a reset generated in this way is not device specific. All devices on the same I2C bus that support the general call mode will perform a reset. Additionally, this command only works when the sensor is able to process I2C commands. The appropriate command consists of two bytes and is shown in Table 13.

Command	Code
Address byte	0x00
Second byte	0x06
Reset command using the general call address	0x0006

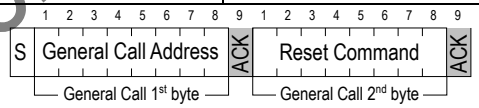


Table 13: Reset through the general call address (Clear blocks are controlled by the microcontroller, grey blocks by the sensor).

Hard Reset

A hard reset is achieved by switching the supply voltage to the VDD Pin off and then on again. In order to prevent powering the sensor over the ESD diodes, the voltage to pins 1 (SCL) and 4 (SDA) also needs to be removed.

4.10 Heater

The SHT85 is equipped with an internal heater, which is meant for plausibility checking only. The temperature increase achieved by the heater depends on various parameters and lies in the range of a few degrees centigrade. It can be switched on and off by command, see table below. The status is listed in the status register. After a reset the heater is disabled (default condition).

Command	Hex Code	
	MSB	LSB
Heater Enable	0x30	6D
Heater Disabled		66

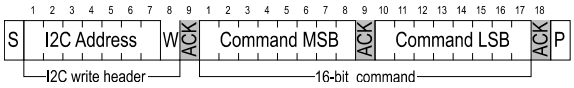


Table 14: Heater command (Clear blocks are controlled by the microcontroller, grey blocks by the sensor).

4.11 Status Register

The status register contains information on the operational status of the heater, the alert mode and on the execution status of the last command and the last write sequence. The command to read out the status register is shown in Table 15 whereas a description of the content can be found in Table 16.

Command	Hex code
Read Out of status register	0xF32D

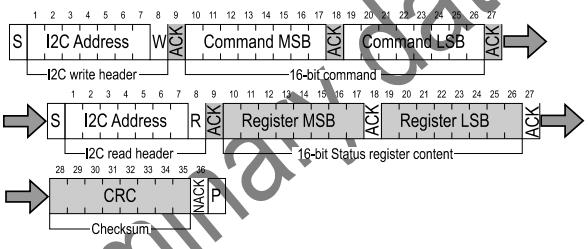


Table 15: Command to read out the status register (Clear blocks are controlled by the microcontroller, grey blocks by the sensor).

Bit	Field description	Default value
15	Alert pending status '0': no pending alerts '1': at least one pending alert	'1'
14	Reserved	'0'
13	Heater status '0' : Heater OFF '1' : Heater ON	'0'
12	Reserved	'0'
11	RH tracking alert '0' : no alert '1' . alert	'0
10	T tracking alert '0' : no alert '1' . alert	'0'
9:5	Reserved	'xxxxx'
4	System reset detected '0': no reset detected since last 'clear status register' command '1': reset detected (hard reset, soft reset command or supply fail)	'1'
3:2	Reserved	'00'
1	Command status '0': last command executed successfully '1': last command not processed. It was either invalid, failed the integrated command checksum	'0'
0	Write data checksum status '0': checksum of last write transfer was correct '1': checksum of last write transfer failed	'0'

Table 16: Description of the status register.

Clear Status Register

All flags (Bit 15, 11, 10, 4) in the status register can be cleared (set to zero) by sending the command shown in Table 17.

Command	Hex Code
Clear status register	0x 30 41

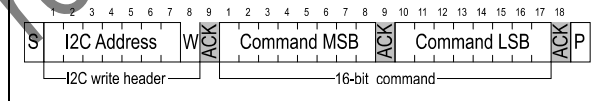


Table 17: Command to clear the status register (Clear blocks are controlled by the microcontroller, grey blocks by the sensor).

4.12 Checksum Calculation

The 8-bit CRC checksum transmitted after each data word is generated by a CRC algorithm. Its properties are displayed in Table 18. The CRC covers the contents of the two previously transmitted data bytes. To calculate the checksum only these two previously transmitted data bytes are used.

Property	Value
Name	CRC-8
Width	8 bit
Protected data	read and/or write data
Polynomial	0x31 ($x^8 + x^5 + x^4 + 1$)
Initialization	0xFF
Reflect input	False
Reflect output	False
Final XOR	0x00
Examples	CRC (0xBEEF) = 0x92

Table 18: I2C CRC properties.

4.13 Conversion of Signal Output

Measurement data is always transferred as 16-bit values (unsigned integer). These values are already linearized and compensated for temperature and supply voltage effects. Converting those raw values into a physical scale can be achieved using the following formulas.

Relative humidity conversion formula (result in %RH):

$$RH = 100 \cdot \frac{S_{RH}}{2^{16} - 1}$$

Temperature conversion formula (result in °C & °F):

$$T[°C] = -45 + 175 \cdot \frac{S_T}{2^{16} - 1}$$

$$T[°F] = -49 + 315 \cdot \frac{S_T}{2^{16} - 1}$$

S_{RH} and S_T denote the raw sensor output for humidity and temperature, respectively. The formulas work only correctly when S_{RH} and S_T are used in decimal representation.

4.14 Communication Timing

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
SCL clock frequency	f_{SCL}		0	-	1000	kHz	
Hold time (repeated) START condition	$t_{HD;STA}$	After this period, the first clock pulse is generated	0.24	-	-	µs	
LOW period of the SCL clock	t_{LOW}		0.53	-	-	µs	
HIGH period of the SCL clock	t_{HIGH}		0.26	-	-	µs	
SDA hold time	$t_{HD;DAT}$		0	-	250	ns	Transmitting data
			0	-	- -	ns	Receiving data
SDA set-up time	$t_{SU;DAT}$		100	-	-	ns	
SCL/SDA rise time	t_R		-	-	300	ns	
SCL/SDA fall time	t_F		-	-	300	ns	
SDA valid time	$t_{VD;DAT}$		-	-	0.9	µs	
Set-up time for a repeated START condition	$t_{SU;STA}$		0.26	-	-	µs	
Set-up time for STOP condition	$t_{SU;STO}$		0.26	-	-	µs	
Capacitive load on bus line	CB		-	-	400	pF	
Low level input voltage	V_{IL}		0	-	0.3xV_{DD}	V	
High level input voltage	V_{IH}		0.7xV_{DD}	-	1xV_{DD}	V	
Low level output voltage	V_{OL}	33 mA sink current	-	-	0.4	V	

Table 19: Timing specifications for I2C communication, valid for T=-40°C… 125°C and VDD = VDDmin… VDDmax. The nomenclature above is according to the I2C Specification (UM10204, Rev. 6, April 4, 2014).

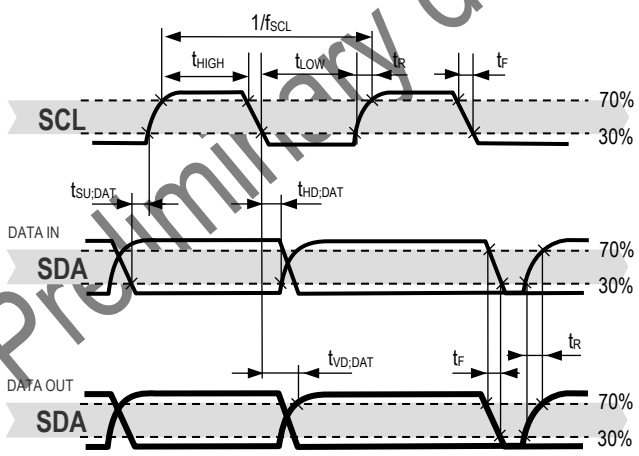


Figure 5: Timing diagram for digital input/output pads. SDA directions are seen from the sensor. Bold SDA lines are controlled by the sensor, plain SDA lines are controlled by the micro-controller. Note that SDA valid read time is triggered by falling edge of preceding toggle.

5 Packaging

The SHT85 is supplied in a single-in-line pin type package. The SHT35-DIS sensor housing consists of an epoxy-based mold compound, see “Datasheet SHT3x-DIS” for more information. The sensor opening of the housing is protected by a PTFE membrane dedicated to protect the sensor opening from liquids and dust according to IP67, see “Datasheet Membrane Option” for more information. The sensor head is connected to the pins by a small bridge to minimize heat conduction and response times. The pins are soldered to the FR4 substrate by lead-free solder paste. The gold plated backside of the sensor head is connected to the VSS pin. A 100nF capacitor is mounted on the front side between VDD and VSS. The device is fully RoHS compliant – thus it is free of of Pb, Cd, Hg, Cr(6+), PBB and PBDE. All pins are Au plated to avoid corrosion. They can be soldered or mate with most 1.27 mm (0.05”) sockets, for example: Preci-dip / Mill-Max R851-83-004-20-001 or similar. When the sensor is further processed by soldering, it should be ensured that the solder connections between pins and the SHT85 PCB are not melted.

5.1 Traceability

The SHT85 provides a device specific serial number, which can be read-out via the serial interface (I2C), see the command in Table 20. The Serial number allows an unambiguous identification of each individual device.

Command	Hex Code
Get Serial Number	0x 36 82

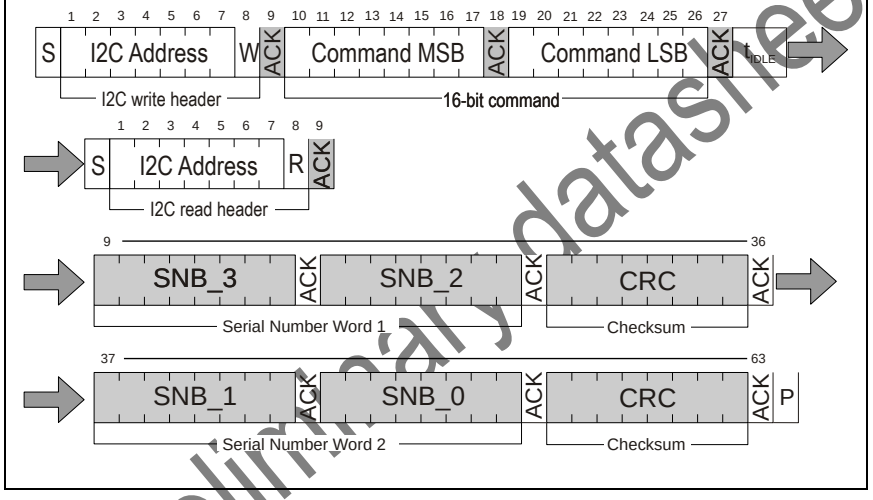


Table 20: Command to read out the Serial Number (Clear blocks are controlled by the microcontroller, grey blocks by the sensor.)

After issuing the measurement command and sending the ACK Bit the sensor needs the time t_{IDLE} = 0.5ms to respond to the I2C read header with an ACK Bit. Hence it is recommended to wait t_{IDLE} =0.5ms before issuing the read header. The Get Serial Number command returns 2 words; every word is followed by a CRC Checksum. Together the 2 words (SNB_3 to SNB_0 in Table 20, SNB_0 is the LSB, whereas SNB_3 is the MSB) constitute a unique serial number with a length of 32 bit. This serial number can be used to identify each sensor individually.

5.2 Package Outline

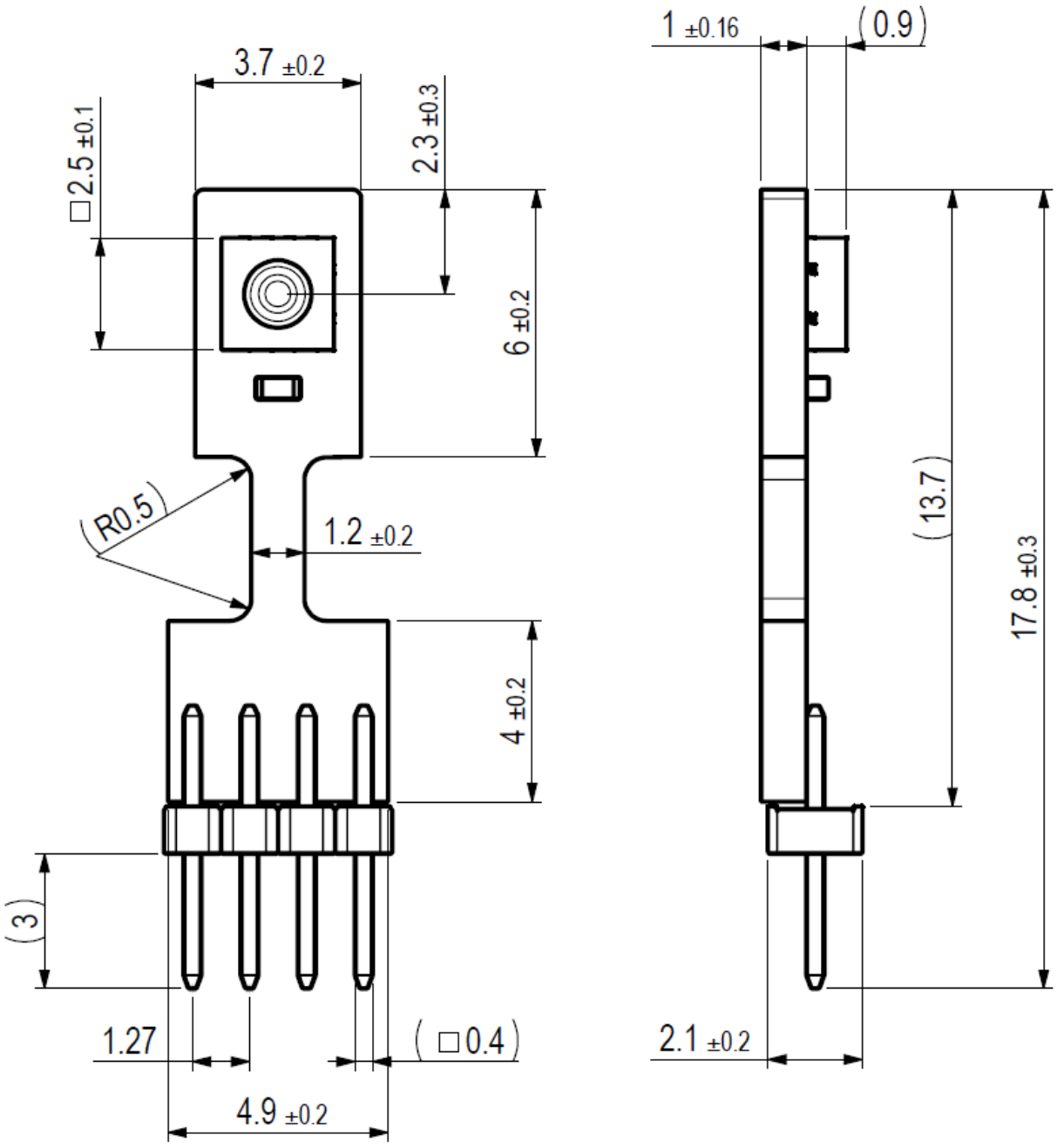
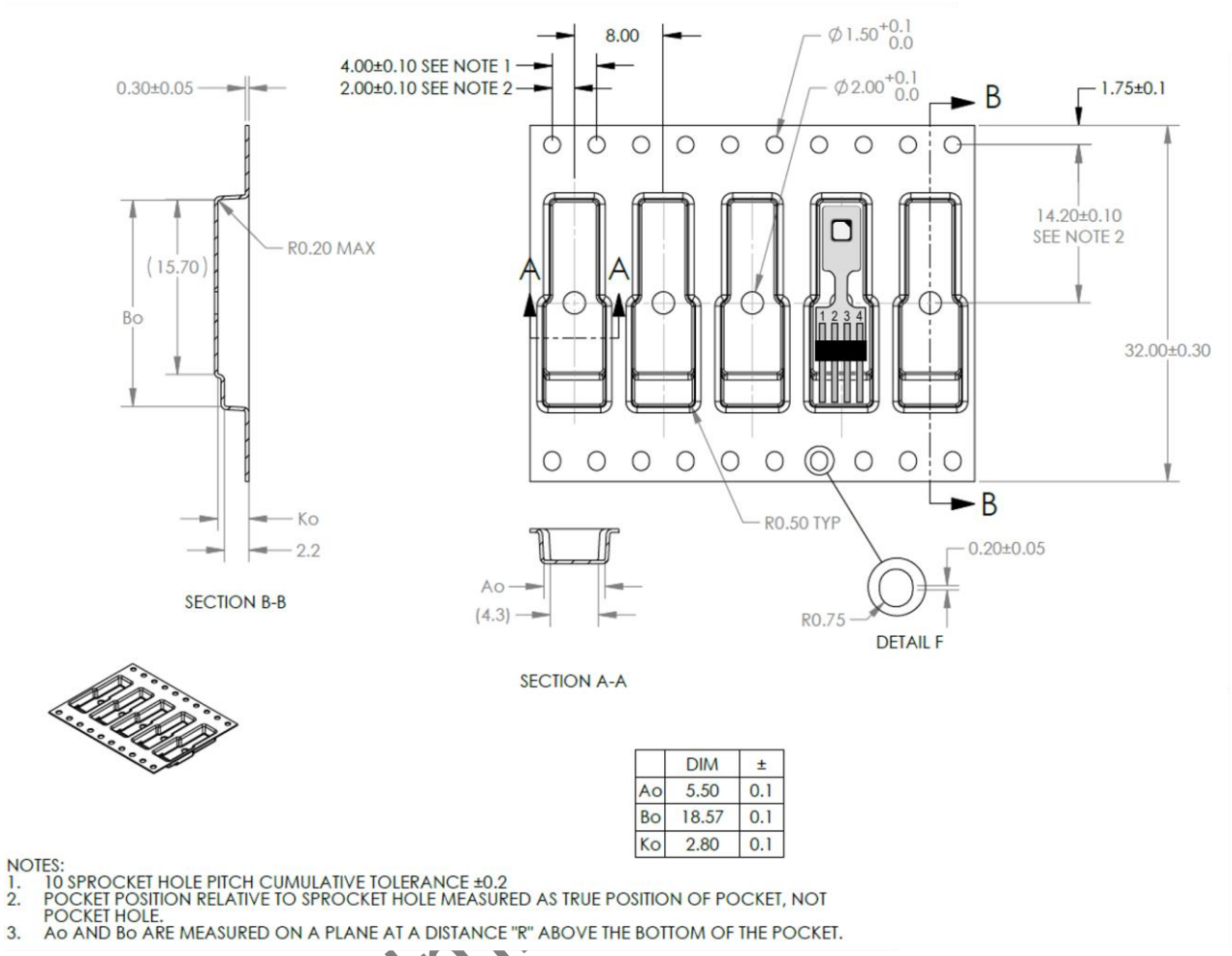


Figure 6: Dimensional drawing of the SHT85 sensor packaging. Dimensions are in mm (1mm = 0.039 inch).

6 Shipping Package

SHT85 are shipped in 32mm tape at 50pcs each. Dimensions of packaging tape are given in Figure 7. All tapes have a 10 pockets empty leader tape (first pockets of the tape) and a 10 pockets empty trailer tape (last pockets of the tape).



	DIM	±
Ao	5.50	0.1
Bo	18.57	0.1
Ko	2.80	0.1

NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.
3. Ao AND Bo ARE MEASURED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

Figure 7 Tape configuration and unit orientation within tape, dimensions in mm (1mm = 0.039inch).

7 Quality

Qualification of the SHT85 is performed based on JEDEC guidelines. Furthermore, the SHT3x-DIS component qualification is based on the AEC Q 100 qualification test method.

7.1 Material Contents

The device is fully RoHS compliant, e.g. free of Pb, Cd, and Hg.

8 Ordering Information

The SHT85 can be ordered in tape and reel packaging, see Table 21. The reels are sealed into antistatic ESD bags.

Sensor Type	Packaging	Quantity	Order Number
SHT85	Tape Stripes	50	3.000.074

Table 21 SHT85 ordering information.

9 Further Information

For more in-depth information on the SHT85 and its application please consult the documents in Table 22. Parameter values specified in the datasheet overrule possibly conflicting statements given in references cited in this datasheet.

Document Name	Description	Source
SHT85 Shipping Package	Describes the standard shipping package	Available upon request.
Handling of SMD Packages Humidity Sensors	Assembly Guide	Available for download at the Sensirion humidity sensors download center: www.sensirion.com/humidity-download
Datasheet Humidity Sensor SHT3x Digital	All specifications of the SHT35-DIS	Available for download at the Sensirion humidity sensors download center: www.sensirion.com/humidity-download
Datasheet Humidity Sensor Filter Membrane SHT3x	All relevant specifications of the filter membrane	Available for download at the Sensirion humidity sensors download center: www.sensirion.com/humidity-download
Handling Instructions Humidity Sensors	Guidelines for proper handling of SHTxx humidity sensors	Available for download at the Sensirion humidity sensors download center: www.sensirion.com/humidity-download
Specification Statement Humidity Sensors	Definition of sensor specifications.	Available for download at the Sensirion humidity sensors download center: www.sensirion.com/humidity-download

Table 22 Documents containing further information relevant for the SHT85.

10 Important Notices

10.1 Warning, Personal Injury

Do not use this product as safety or emergency stop devices or in any other application where failure of the product could result in personal injury. Do not use this product for applications other than its intended and authorized use. Before installing, handling, using or servicing this product, please consult the data sheet and application notes. Failure to comply with these instructions could result in death or serious injury.

If the Buyer shall purchase or use SENSIRION products for any unintended or unauthorized application, Buyer shall defend, indemnify and hold harmless SENSIRION and its officers, employees, subsidiaries, affiliates and distributors against all claims, costs, damages and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if SENSIRION shall be allegedly negligent with respect to the design or the manufacture of the product.

10.2 ESD Precautions

The inherent design of this component causes it to be sensitive to electrostatic discharge (ESD). To prevent ESD-induced damage and/or degradation, take customary and statutory ESD precautions when handling this product.
See application note "ESD, Latchup and EMC" for more information.

10.3 Warranty

SENSIRION warrants solely to the original purchaser of this product for a period of 12 months (one year) from the date of delivery that this product shall be of the quality, material and workmanship defined in SENSIRION's published specifications of the product. Within such period, if proven to be defective, SENSIRION shall repair and/or replace this product, in SENSIRION's discretion, free of charge to the Buyer, provided that:

- notice in writing describing the defects shall be given to SENSIRION within fourteen (14) days after their appearance;
- such defects shall be found, to SENSIRION's reasonable satisfaction, to have arisen from SENSIRION's faulty design, material, or workmanship;
- the defective product shall be returned to SENSIRION's factory at the Buyer's expense; and
- the warranty period for any repaired or replaced product shall be limited to the unexpired portion of the original period.

This warranty does not apply to any equipment which has not been installed and used within the specifications recommended by SENSIRION for the intended and proper use of the equipment. EXCEPT FOR THE WARRANTIES EXPRESSLY SET FORTH HEREIN, SENSIRION MAKES NO WARRANTIES, EITHER EXPRESS OR IMPLIED, WITH RESPECT TO THE PRODUCT. ANY AND ALL WARRANTIES, INCLUDING WITHOUT LIMITATION, WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, ARE EXPRESSLY EXCLUDED AND DECLINED.
SENSIRION is only liable for defects of this product arising under the conditions of operation provided for in the data sheet and proper use of the goods. SENSIRION explicitly disclaims all warranties, express or implied, for any period during which the goods are operated or stored not in accordance with the technical specifications.
SENSIRION does not assume any liability arising out of any application or use of any product or circuit and specifically disclaims any and all liability, including without limitation consequential or incidental damages. All operating parameters, including without limitation recommended parameters, must be validated for each customer's applications by customer's technical experts. Recommended parameters can and do vary in different applications.
SENSIRION reserves the right, without further notice, (i) to change the product specifications and/or the information in this document and (ii) to improve reliability, functions and design of this product.

11 Revision History

Release Date	Version	Page(s)	Changes
28 September 2018	0.9	All	Initial Preliminary Release

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VH400 Soil Moisture Sensor Probes

1 . Information

Our VH400 series soil moisture sensor probes enable precise low cost monitoring of soil water content.

Because our probe measures the dielectric constant of the soil using transmission line techniques, it is insensitive to water salinity, and will not corrode over time as does conductivity based probes. Our probes are small, rugged, and low power.

Compared to other low cost sensor such as gypsum block sensors, our probes offer a rapid response time. They can be inserted and take an accurate reading in under a second.
Probes come in standard cable lengths of 2 meters, 5 meters and 10 meters.

2 . Soil Moisture Sensor Probe Applications

- Irrigation and sprinkler systems.
- Moisture monitoring of bulk foods.
- Rain and weather monitoring.
- Environmental monitoring.
- Water conservation applications.

3 . Soil Moisture Sensor Probe Features

- Extreme low cost with volume pricing.
- Not conductivity based.
- Insensitive to salinity.
- Probe does not corrode over time.
- Rugged design for long term use.
- Small size.
- Consumes less than 7mA for very low power operation.
- Precise measurement.
- Measures volumetric water content (VWC) or gravimetric water content (GWC).
- Output Voltage is proportional to moisture level.
- Wide supply voltage range.
- Can be buried and is water proof.
- Probe is long and slender for wider use, including smaller potted plants.

4 . Soil Moisture Sensor Probe Ordering Info

ORDER INFO

Part Number	Description
VH400-2M	Soil Moisture Sensor - 2 meter cable
VH400-5M	Soil Moisture Sensor - 5 meter cable
VH400-10M	Soil Moisture Sensor - 10 meter cable

5 . Soil Moisture Sensor Relay Boards

The quickest way to evaluate if the VH400 series is right for you is to also order some of our sensor relay boards. The relay boards accept input from a single sensor and control a solid state or mechanical relay.

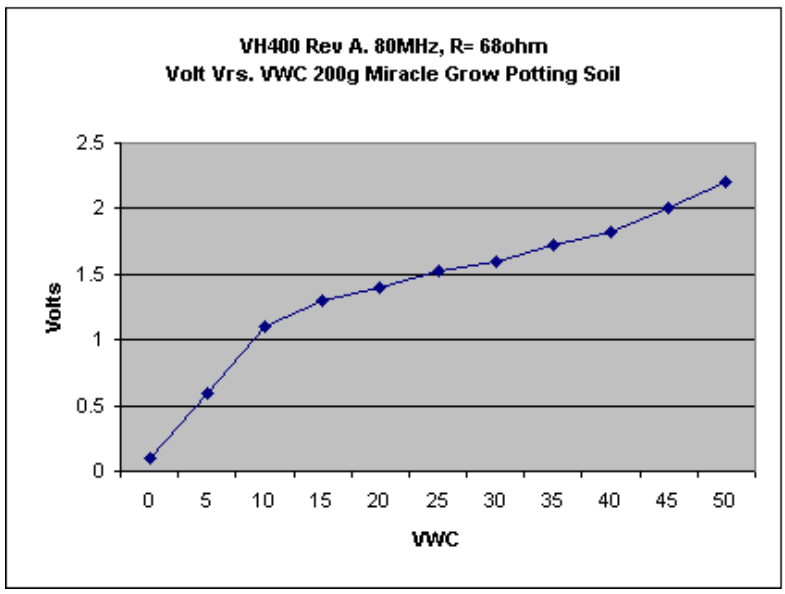
The relay contacts can be configured to close when wet, or open when wet. The dry/wet threshold is easily set by an an on boardvariable resistor, which can be tuned with a small screwdriver. With our relay boards, within minutes you'll be using your VH400 soil moisture probe to control, valves, alarms or home automation systems.

6 . Soil Moisture Sensor Probe Specifications

Power consumption	< 13mA
Supply Voltage	3.5V to 20 VDC.
Dimensions	See drawing below.
Power on to Output stable	400 ms
Output Impedance	10K ohms
Operational Temperature	-40ºC to 85ºC
Accuracy	2% at 25˚C
Output	0 to 3V related to moisture content
Shell Color	Red

6.1) Figure 1: VH400 Rev A to Rev G: VWC to Voltage Curves

VWC to Voltage curve for container with 200g of Miracle Grow Potting Soil.



6.2) VH400 Piecewise Curve

Most curves can be approximated with linear segments of the form:

y= m*x-b,

where m is the slope of the line

The VH400's Voltage to VWC curve can be approximated with 4 segents of the form:

VWC= m*V-b

where V is voltage.

m= (VWC2 - VWC1)/(V2-V1)

where V1 and V2 are voltages recorded at the respective VWC levels of VWC1 and VWC2.

After m is determined, the y-axis intercept coefficient b can be found by inserting one of the end points into the equation:

b= m*v-VWC

Voltage Range	Equation
0 to 1.1V	VWC= 10*V-1
1.1V to 1.3V	VWC= 25*V- 17.5
1.3V to 1.82V	VWC= 48.08*V- 47.5
1.82V to 2.2V	VWC= 26.32*V- 7.89

7. Soil Moisture Sensor Probe Wiring Table

Color	Description
Bare	Ground
Red	POWER: 3.5V to 20 VDC.
Black	OUT: (0 to 3V related to moisture content.)

8. VH400 Soil Moisture Sensor Probe Drawing